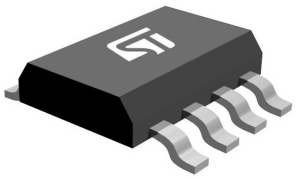
STPW12

Datasheet

Programmable electronic power breaker for 12 V bus



Power SO8

Features

- Real-time input power sensing
- Input voltage range: from 10.5 V to 18 V
- Continuous current typ.: 1.5 A
- P-channel on resistance typ.: 50 mΩ
- Power limit accuracy typ.: 3%
- Undervoltage lockout
- Adjustable power limitation
- PWM mode
- Programmable power limit masking time
- Programmable auto-retry delay
- Thermal shutdown
- Enable function
- Short-circuit current limit
- Operative junction temp. - 40 °C to 125 °C
- Available in power SO8 package
- Simplifies UL compliance and certification

Applications

- White goods
- Consumer electronics
- Industrial applications
- Air contidioner
- User interface
- Fan motor control

Maturity status link	
STPW12	
Device summary	
Order code	STPW12PHR
Package	Power SO8

Description

The STPW12 is an integrated electronic power breaker, optimized to monitor the input power.

Connected in series to the power rail, it is able to disconnect the electronic circuitry on its output if the power consumption overcomes the programmed limit. When this happens, the device automatically opens the integrated power switch and disconnects the load.

The intervention of the protection is communicated to the board monitoring circuits through a signal on the fault pin.

After a certain delay time, programmable by the user, the device automatically tries again to close the internal switch and re-connect the load.

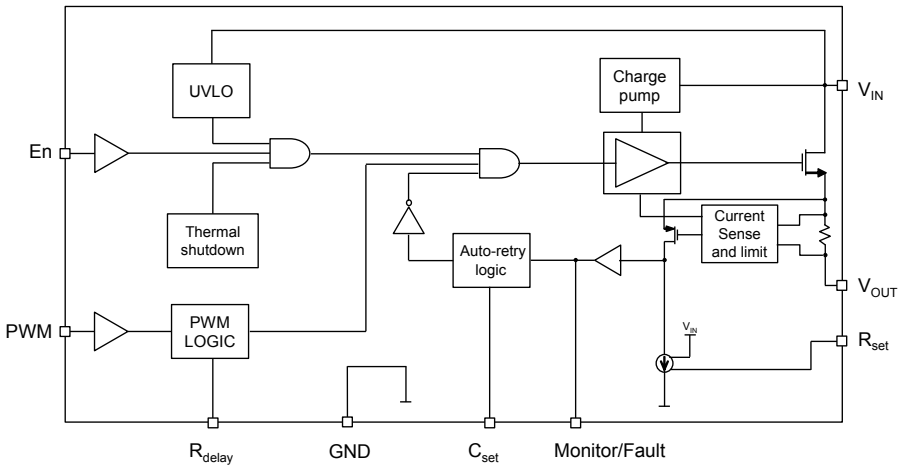
A dedicated monitor pin provides the user with continuous information on the monitored power.

The device can be enabled/disabled through a dedicated pin, and a direct PWM mode can be implemented providing PWM pin with an external signal.

This approach allows the user to optimize the design power distribution system, in terms of accurate power control, choice of isolation material, safety improvement, such as: reduced risk of flammability and easier qualification and certification flow.

1 Diagram

Figure 2. **Block diagram**



2 Pin configuration

Figure 3. **Pin connection (top view)**

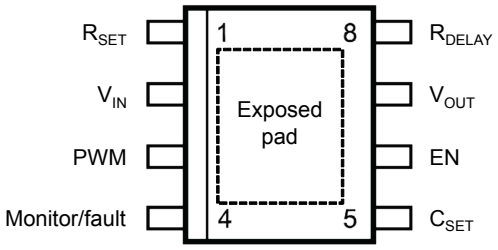


Table 1. **Pin description**

Pin n°	Symbol	Note
1	R_{SET}	An R_S resistor between this pin and GND fixes the power limiting threshold
2	V_{IN}	Input voltage
3	PWM	A PWM signal can be provided through this pin to turn-ON/OFF the power switch If PWM function is not used it is suggested to connect this pin to EN or V_{IN}
4	Monitor/fault	Power monitor signal, fault signal
5	C_{SET}	A C_S capacitor between this pin and GND sets the auto-retry delay
6	Enable	Enable pin (device active when EN=high)
7	V_{OUT}	Output pin
8	R_{delay}	An R_D resistor connected between this pin and GND sets the power limit masking time. Do not connect this pin directly to GND
Exp.pad	GND	Device GND connection

3 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	Positive power supply voltage	-0.3 to 25	V
V_{OUT}	Output voltage	-0.3 to V_{IN} + 0.3	V
R_{set}	R_{set} pin voltage	-0.3 to 7	V
C_{set}	C_{set} pinvoltage	-0.3 to 7	V
R_{delay}	R_{delay} pin voltage	-0.3 to 7	V
Monitor/fault	Monitor/fault pin voltage	-0.3 to 7	V
I_D	Continuous current	Internally limited	A
T_J	Operating junction temperature range (1)	-40 to 125	°C
T_{STG}	Storage temperature range	-65 to 150	°C
T_{LEAD}	Lead temperature (soldering) 10 s	260	°C

1. *The thermal shutdown limit is set above the maximum thermal ratings. It is not recommended to operate the device at temperatures greater than the maximum ratings for extended periods of time.*

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	40	°C/W
R_{thJC}	Thermal resistance junction-case	12	°C/W

4 Electrical characteristics

V_{IN} = 12 V, V_{EN} = V_{PWM} = 5 V, C_I = 10 µF, C_O = 10 µF, T_J = 25 °C (unless otherwise specified).

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage range	V_{PWM} = V_{IN}	10.5		18	V
Under/overvoltage protection						
V_{UVLO}	Undervoltage lockout	Turn-on, voltage going up, I_{LOAD} = 5 mA		8.1		V
V_{Hyst}	UVLO hysteresis	I_{LOAD} = 5 mA		2.2		V
Power MOSFET						
R_{DSon}	ON-resistance	*Note: Pulsed test.*		50	70	mΩ
Power limit circuit						
ΔP	Power limit accuracy	Limit set to 15 W, R_S = 2.7 kΩ V_{IN} = 12 V, T_J = 25 °C		±3		%
		Limit set to 15 W, V_{IN} = 12 V, T_J = 0 to 75 °C (1)	-7.5		+7.5	
P	Power limit range		10		16	W
Enable						
V_{IL}	Low level input voltage	Output disabled			0.8	V
V_{IH}	High level input voltage	Output enabled	2			V
I_{EN}	Enable pin current	V_{EN} = 12 V		0.1	1	µA
PWM input logic						
V_{SPL}	Low level input voltage	Turn-off			0.8	V
V_{SPH}	High level input voltage	Turn-on	2			V
I_{PWM}	PWM pin current	V_{PWM} = 12 V		0.1	1	µA
f_{PWM}	PWM signal frequency	No C_{OUT}		2		kHz
D	PWM signal duty cycle	No C_{OUT}	20		100	%
Auto-retry circuit						
I_{SET}	C_S capacitor charging current	During fault condition		0.16		µA
Power limit masking circuit						
t_{mask}	Masking time in PWM mode	R_D = 1 kΩ		45		µs
Total device						
I_{Bias}	Bias current	R_S = 2.7 kΩ device operational		4		mA
		Shutdown mode		40	100	µA
Thermal shutdown						
TSD	Shutdown temperature	(2)		160		°C
	Hysteresis			15		

1. *Values over the temperature range are guaranteed by design/correlation and tested in production only at ambient temperature.*
2. *Guaranteed by design, but not tested in production.*

5 Typical application diagram

Figure 4. **Application circuit**

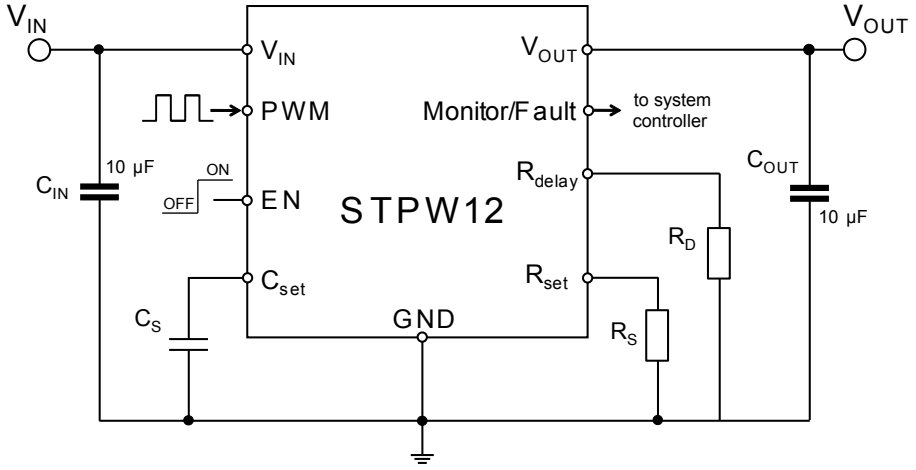
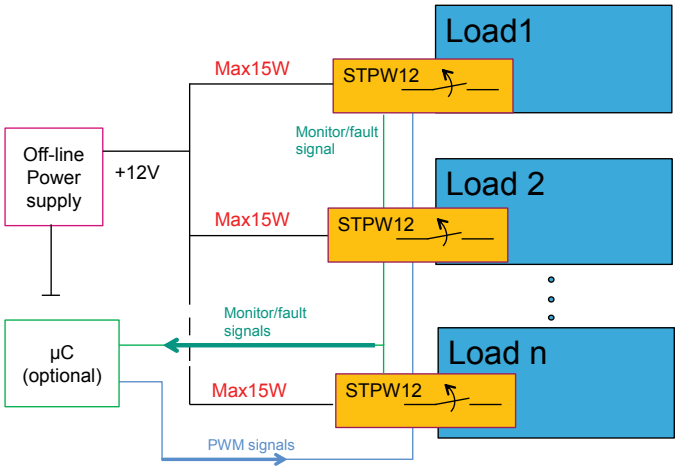


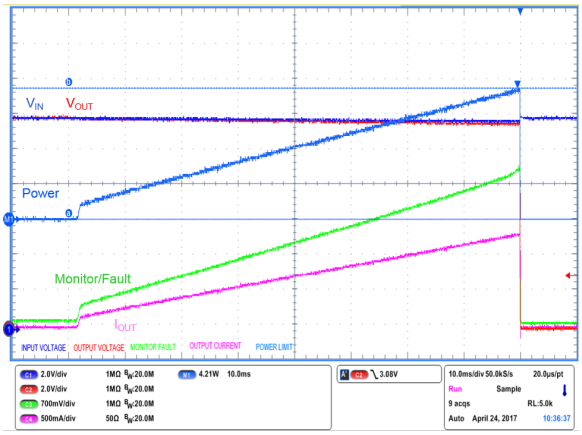
Figure 5. **Application diagram**



6 Typical characteristics

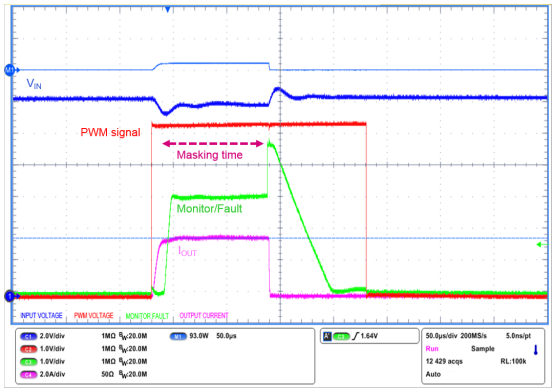
V_{IN} = 12 V, I_{LOAD} = 1 A, V_{EN} = V_{PWM} = 5 V, C_I = 10 µF, C_O = 10 µF, T_J = 25 °C (unless otherwise specified).

Figure 6. Monitor signal vs. power



V_{IN} = 12V, C_{IN} = 22 µF, C_{OUT} = 10 µF, I_{OUT} = from 0 to power limit

Figure 7. Masking time, fault signal



V_{IN} = 12 V C_{IN} = 10 µF, C_{OUT} = 68 nF, EN = V_{IN}, R_{DELAY} = 10 kΩ, PWM from 0 to 5 V

Figure 8. On resistance vs. temperature

V_{IN} = 12 V, C_{IN} = 10 µF, C_{OUT} = 10 µF I_{OUT} = from 0.5 A

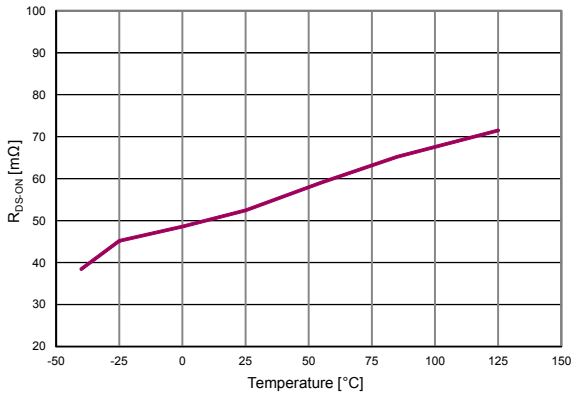


Figure 9. UVLO thresholds vs. temperature

V_{IN} = from 5 V to 12 V and back, I_{OUT} = 50 mA, EN = PWM = V_{IN}

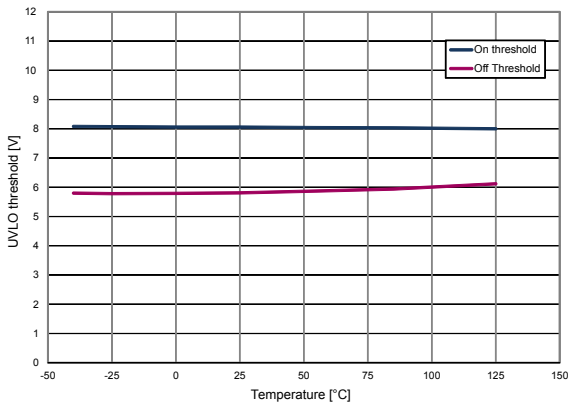


Figure 10. Enable thresholds vs. temperature

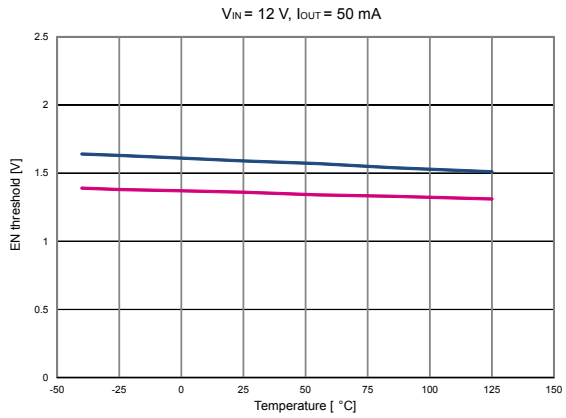


Figure 11. PWM thresholds vs. temperature

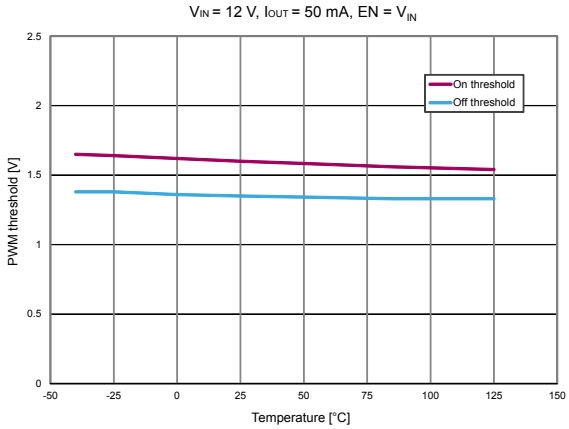


Figure 12. Bias current vs. temperature

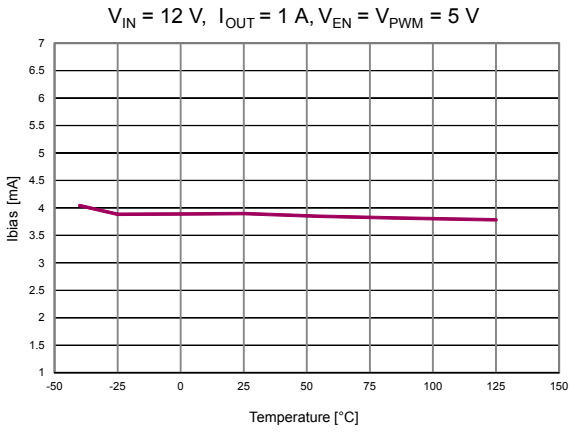


Figure 13. Off-state current vs. temperature

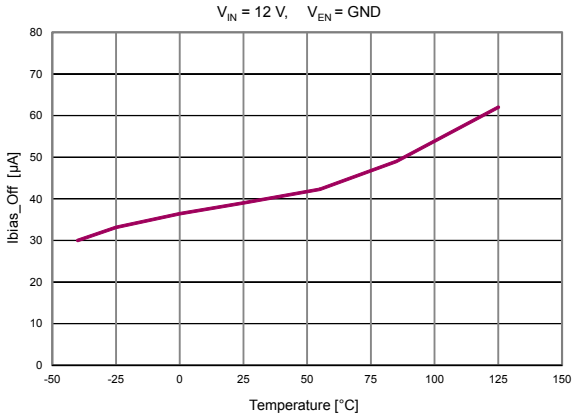


Figure 14. Power limit accuracy vs. temperature

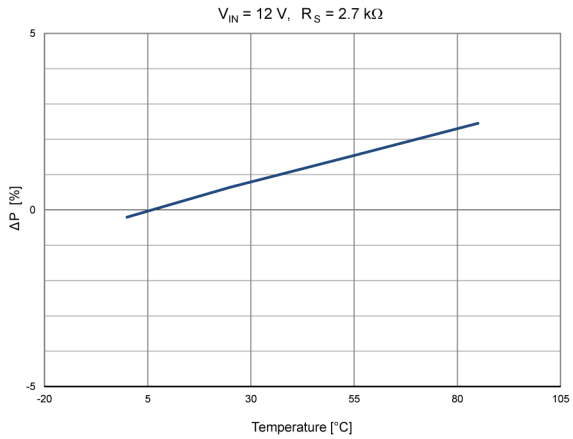


Figure 15. Power limit threshold vs. R_S

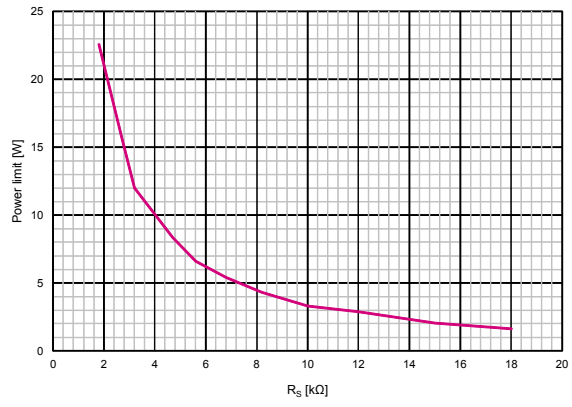


Figure 16. Auto-retry delay time vs. C_S

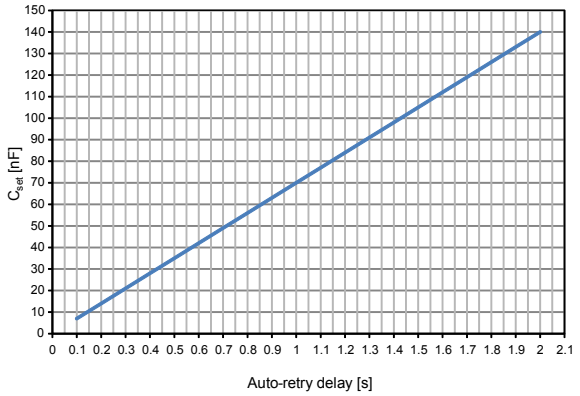
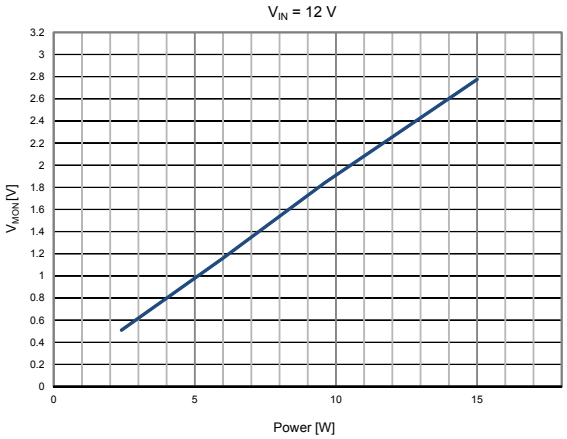


Figure 17. Monitor voltage vs. power



7 The STPW12 detailed description

7.1 Power breaker intervention and thermal shutdown

The device disconnects the load if the power overcomes the pre-set threshold.

The intervention threshold is programmed by the R_s resistor, connected by the R_{set} pin and GND. The R_s resistor can be chosen with the help of the Figure 15. Power limit threshold vs. R_S graph and can be rated for ¼ W.

The accuracy level of the limiting circuit is achieved by using high precision resistor (0.1%) for the R_s. The lower precision resistors, the lower precision of the power limit.

The overcoming of the power limit threshold is signalled on the monitor/fault pin (see Figure 7. Masking time, fault signal and Section 7.3 Monitor/fault pin description).

After a programmable delay time, the device attempts again to reconnect the load, by the auto-retry circuit. Each auto-retry cycle starts with the defined masking time.

7.2 Current limit and thermal protections

The STPW12 is equipped with internal self-protections, such as: current limit and thermal shutdown.

Thermal shutdown is always active and occurs if the die temperature reaches the thermal shutdown threshold. If this happens, the device switches off and the load is disconnected. The monitor/fault pin signal goes to low level (power-off).

Once the die temperature decreases to the hysteresis value, the device automatically attempts to restart.

Current limit protection is always active and intervenes in case of strong overload or short-circuit on the output. In such occurrence, the device internal power switch is immediately turned off and the load is disconnected. Therefore the device immediately tries to activate the output. This on-off cycle is repeated until the overload is removed or if thermal protection or power limit are activated.

During current limit events the monitor/fault pin is set to high logic level (4.5 V typ.).

7.3 Monitor/fault pin description

The monitor/fault pin provides two useful signals for the real-time control of the device and application status. A monitor signal proportional to the power is continuously present on the pin. The relation between this signal and the input power is almost linear and it is shown in Figure 6. Monitor signal vs. power and Figure 17. Monitor voltage vs. power.

The target accuracy of monitor signal in relation to the input power is +/-15%, in the typical operating condition (V_{IN} = 12 V, I_{LOAD} = 1 A).

When the power limit threshold is reached, after a settling time t_s of about 30 µs, the monitor/fault pin voltage goes to high logic level for about 10 µs (t_f), so that the user can detect the fault.

Therefore the signal goes to low logic level, the output is turned off and the auto-retry cycle starts.

The same happens if the power limit overcomes during the PWM masking time. See the following pictures and Table 5. Monitor signal truth table for more details.

Figure 18. **Monitor signal vs. power**

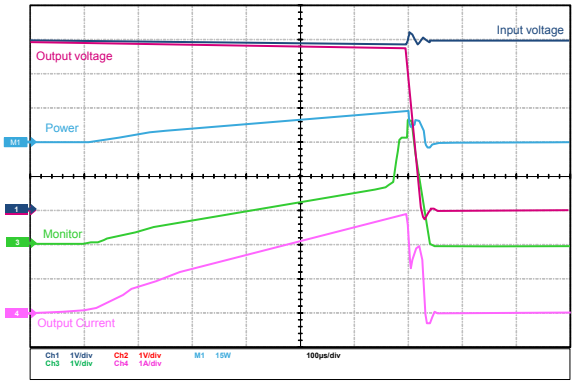


Figure 19. **Monitor signal vs. power (zoom)**

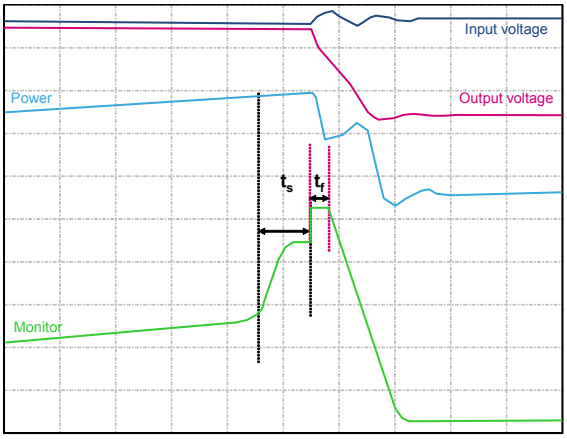


Table 5. **Monitor signal truth table**

Device status	Mon / fault
Normal operation	I_{MON}
Power limit triggered	High (for 10 µs)
Thermal shutdown	Low
Off-state	Low
Current limit triggered	High

The voltage at high logic level is typically 4.5 V, therefore the pin can be directly interfaced to a 5 V compliant microcontroller or ADC device.

7.4 Auto-retry delay time setting

The auto-retry delay time, defined as the time between a power interruption event and the device restart, can be set by choosing the appropriate value for the C_S capacitor, according to the graph in Figure 16. Auto-retry delay time vs. C_S.

7.5 PWM mode description, masking time

In this mode the device internal power switch can be driven on/off by an external PWM signal, provided to the PWM pin (square wave, maximum 2 kHz, duty cycle 20% - 100%). It is important to notice that in this mode the power limit protection is kept inactive for a delay time (masking time) selected by an external R_D resistor (see Table 6. Masking time vs. R_D), so to avoid false triggering during in-rush power events at each PWM signal rising edge.

Eleven discrete steps are available for the PWM masking time. They can be selected by choosing an appropriate value of the R_D resistor, as shown in the following table, where the standard 1% resistors are used.

For a correct operation of the device, the R_{Delay} pin must not be directly connected to GND, and the minimum masking time (45 µs) is achieved by using R_D = 1 kΩ.

The masking time is measured starting from when the PWM rising edge overcomes the V_{SPH} threshold till the monitor signal starts increasing (see Figure 7. Masking time, fault signal).

PWM masking time is active also during each start-up cycle (including auto-retry), in order to avoid that inrush current flowing to the output capacitor triggers the power limit, which would cause a premature shutdown.

7.6 Details about the start-up sequence

The device is not equipped with a soft-start control, in order to comply with the maximum PWM frequency, therefore in certain applications, featuring high output capacitance after the device and depending on the load characteristics, the current limit protection could occur during the start-up. The device is immediately turned off and restarted as described in Section 7.2 Current limit and thermal protections. This kind of on-off cycle can happen several times until the C_{OUT} is fully charged and as a result, the start-up is prolonged.

When V_{OUT} reaches the target value, if power limit threshold is overcome and PWM is still high, due to a short masking time the device could turn off. The device then starts again after the auto-retry delay time has elapsed.

For all of the above reasons, R_D and C_S have to be selected carefully in order to achieve the start-up sequence and time that satisfies the needs of the application.

The UVLO internal signal is deglitched by a delay of 60 µs (typ.) after EN assertion, in order to ensure that all the circuit functions are ready for the start-up. UVLO, EN, and PWM signals need being correctly asserted so that the masking time is activated.

During the start-up, attention must be paid in case a specific sequence/connection of V_{IN}, EN and PWM is needed. The following diagrams show two examples of start-up with masking time activation. Figure 20. Start-up with PWM tied to V_{IN} shows a start-up with PWM pin connected directly to V_{IN} (PWM function is not used in the application), whereas Figure 21. Start-up with EN tied to V_{IN} shows a start-up with EN pin tied to V_{IN} (EN function is not used in the application).

Figure 20. Start-up with PWM tied to V_{IN}

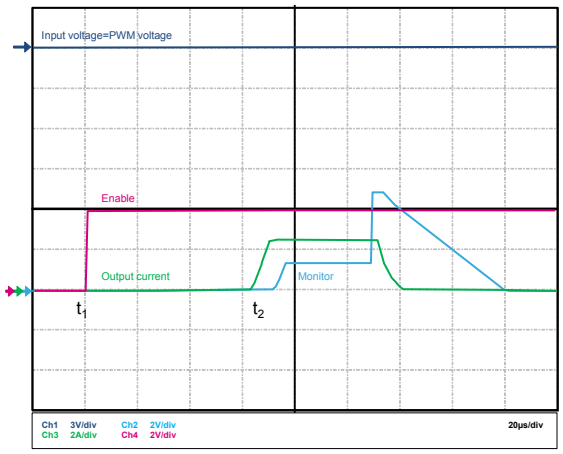
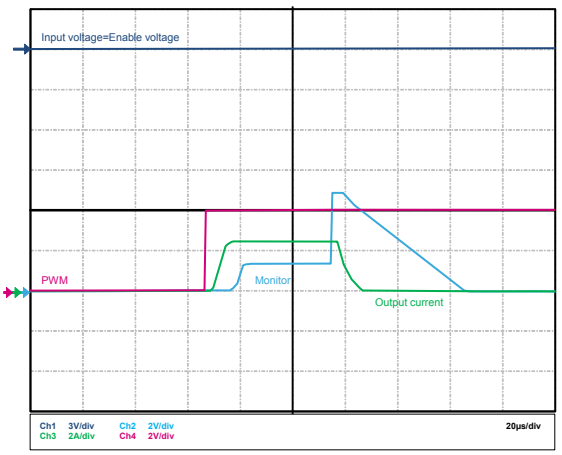


Figure 21. Start-up with EN tied to V_{IN}



With reference to Figure 20. Start-up with PWM tied to V_{IN}, at time t_1 the EN signal activates the UVLO comparator and the UVLO deglitch time starts. At deglitch time expiration (t_2) all signals are high, the device is activated and the masking time starts.

Instead, in the case described in Figure 21. Start-up with EN tied to V_{IN}, the enable is applied to V_{IN} connection, so the UVLO deglitch time has already expired when PWM signal is asserted. The masking time starts together with PWM.

Table 6. **Masking time vs. R_D**

R_D [kΩ]	T_{MASK}
1	45 µs
12.7	100 µs
17.8	500 µs
23.2	1 ms
29.4	5 ms
36.5	10 ms
44.2	50 ms
53.6	200 ms
65.5	500 ms
84.5	1000 ms
105 or higher	2000 ms

8 Application guidelines

8.1 Power supply voltage

The device is designed and optimized to work on 12 V power rails, even if the operating supply voltage can range from 10.5 V to 18 V.

The maximum accuracy of the main operating features is reached for an input voltage of 12 V, therefore the operation at lower or higher voltages implies some small variations in the characteristic performance.

8.2 Input and output capacitors

Input and output capacitors are mandatory to guarantee the device control loop stability and reduce the transient effects of stray inductances present in the input and output power paths. In fact when the STPW12 quickly interrupts the current flow due to power limit or thermal shutdown events, input inductance generates a positive voltage spike on the input pin and, at same way, the output inductance generates a negative voltage spike on the output. Such spikes might overcome the absolute maximum voltage ratings of the device and damage the device itself.

To reduce the effects of such transients, C_{IN} capacitor with a minimum value of 10 µF must be connected between the input pin and GND and placed as close as possible to the device. For the same reason, C_{OUT} capacitor has to be connected on the output port. The recommended value is 10 µF, if this is compatible with the required PWM operating frequency.

When the device is supplied via a power line made of very long wires, where input inductance is higher than 3-4 µH, the input capacitance should be increased to 47 µF or more. See also next paragraph for additional information about protection.

8.3 Additional protections and layout guidelines

Recommended additional protections and methods to address the input/output voltage spikes are the following:

– Minimizing inductance of the input and output tracks, by making short and well dimensioned power traces.

– Using TVS diodes on the input to absorb inductive spikes.

– Schottky diode on the output to absorb negative spikes (for instance the STPS2L30).

– Using a ground plane to connect the GND terminal of the IC (exposed pad) to the system GND.

The C_S capacitor, used for the selection of the auto-retry delay time, is charged by a low 160 nA (typ.) current. To minimize the effect of noisy signals present on this PCB on the C_{set} pin, resulting in incorrect delay time, the capacitor should be placed as close as possible to the IC pin and GND.

9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

9.1 Power SO8 package information

Figure 22. Power SO8 package outline

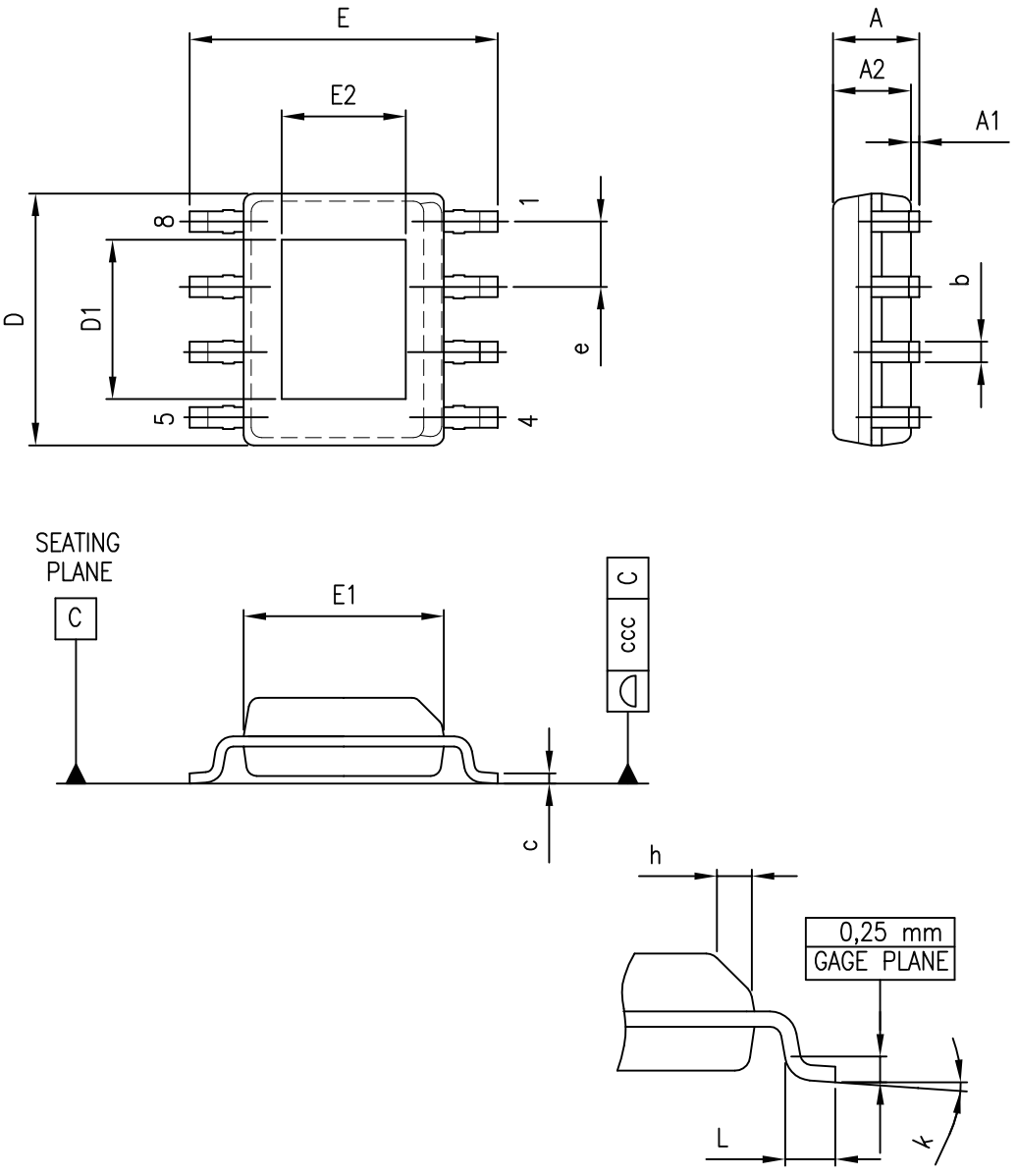


Table 7. **Power SO8 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			1.70
A1	0.00		0.15
A2	1.25		
b	0.38		0.51
c	0.17		0.25
D	4.80	4.90	5.00
D1	3.10	3.30	3.50
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
E2	2.20	2.40	2.60
e		1.27	
h	0.30		0.50
L	0.45	0.60	0.80
k	0		8
ccc			0.10

Figure 23. **Power SO8 recommended footprint**

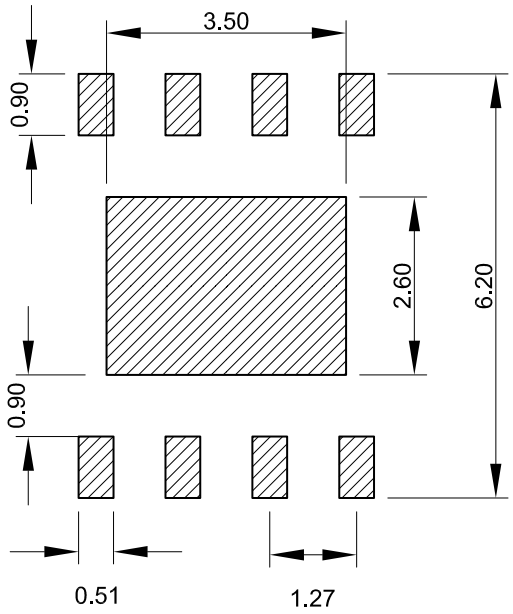
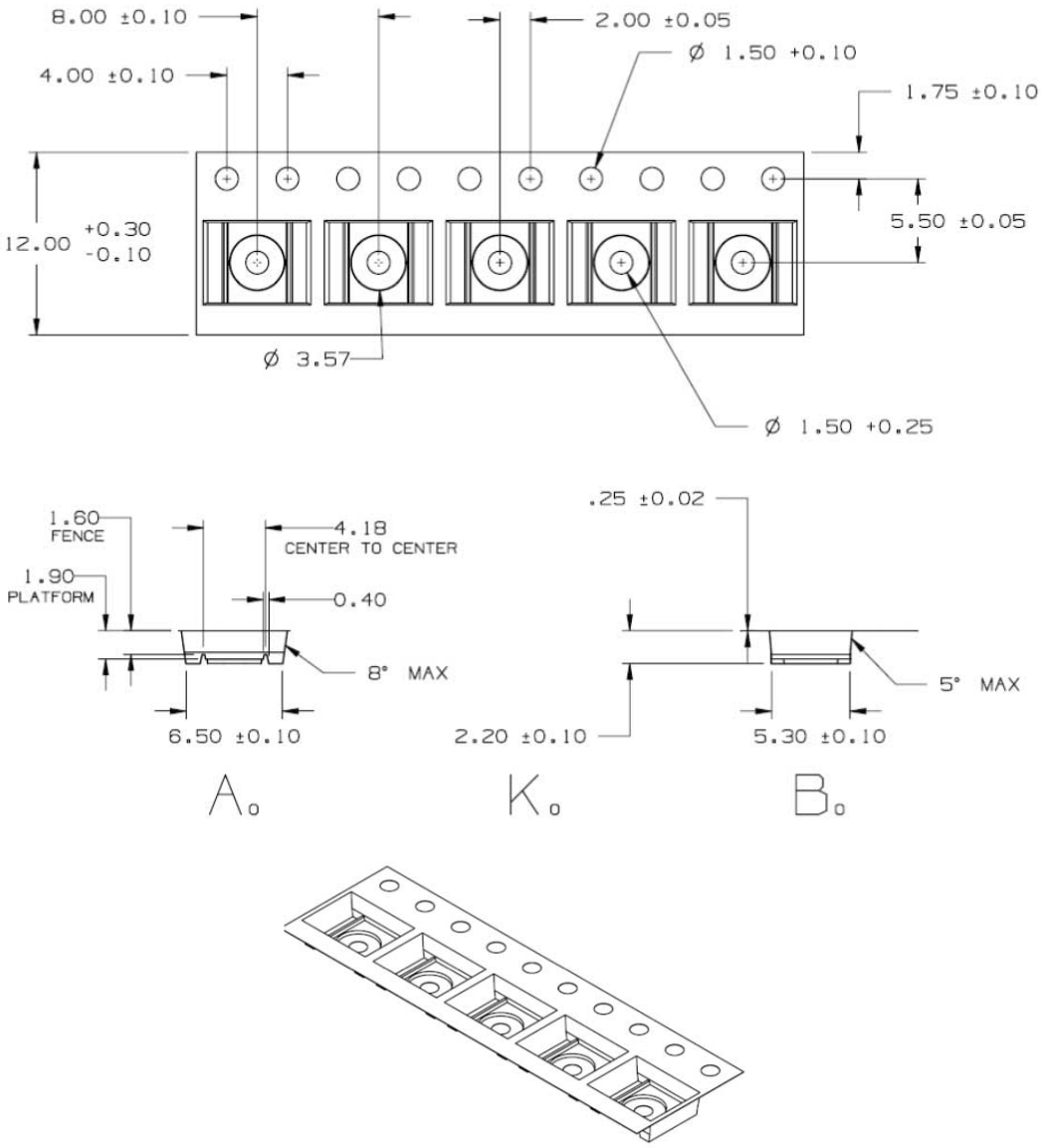


Figure 24. **Power SO8 tape and reel**



Revision history

Table 8. **Document revision history**

Date	Revision	Changes
20-Mar-2018	1	Initial release.

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