# AT24HC04B

## I²C-Compatible (2-Wire) Serial EEPROM
### 4K (512 x 8)

**DATASHEET**

## Features

- Write Protect Pin for Hardware Data Protection
  - Utilizes Different Array Protection Compared to the AT24C04B
- Low-voltage and Standard-voltage Operation
  - 1.8V ($V_{CC}$ = 1.8V to 5.5V)
- Internally Organized 512 x 8 (4K)
- 2-Wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 1MHz (5V) and 400kHz (1.8V, 2.5V, 2.7V) Clock Rate
- 16-byte Page
- Partial Page Writes Allowed
- Self-timed Write Cycle (5ms Max)
- High Reliability
  - Endurance: 1,000,000 Write Cycles
  - Data Retention: 100 Years
- 8-lead PDIP, 8-lead JEDEC SOIC, and 8-lead TSSOP Packages
- Die Sales: Wafer Form, Tape and Reel, and Bumped Wafers

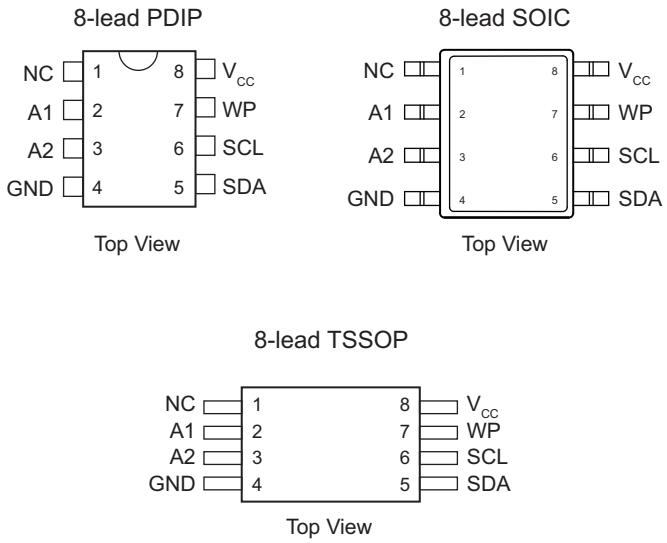
## Description

The Atmel® AT24HC04B provides 4,096 bits of Serial Electrically Erasable and Programmable Read-Only Memory (EEPROM) organized as 512 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The AT24HC04B is available in space-saving 8-lead PDIP, 8-lead JEDEC SOIC, and 8-lead TSSOP packages and is accessed via a 2-wire serial interface. In addition, the entire family is available in 1.8V (1.8V to 5.5V) version.

# 1. Pin Configurations and Pinouts

**Table 1-1. Pin Configuration**

| Pin Name | Function |
|---|---|
| NC | No Connect |
| A1 and A2 | Address Inputs |
| SDA | Serial Data |
| SCL | Serial Clock Input |
| WP | Write Protect |
| $V_{CC}$ | Device Power Supply |




Note: Drawings are not to scale.

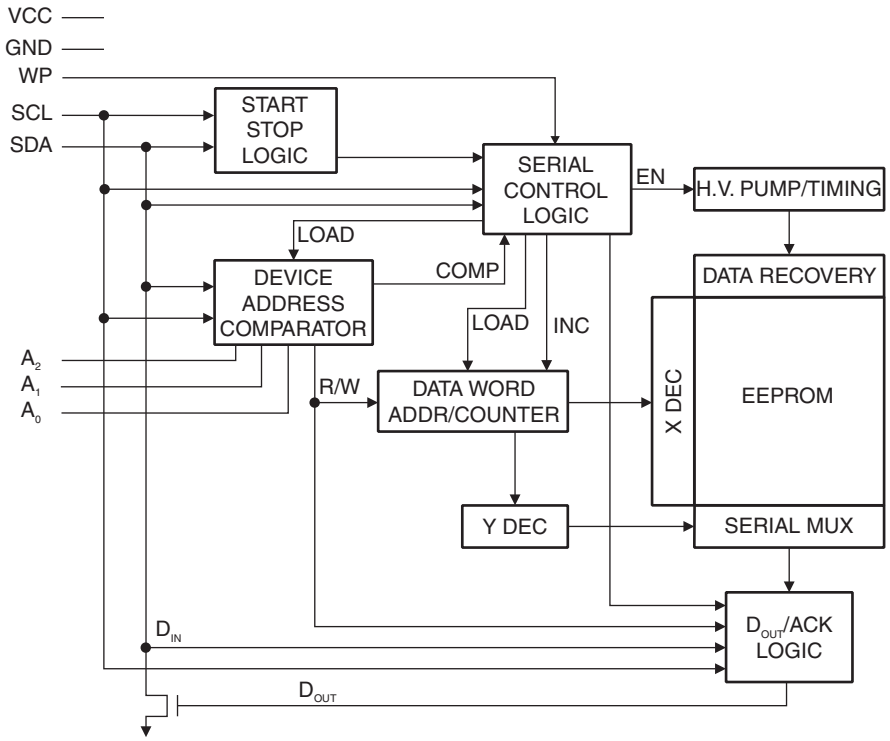
# 2. Absolute Maximum Ratings*

| | |
|---|---|
| Operating Temperature | -40°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| Voltage on Any Pin with Respect to Ground | -1.0V to +7.0V |
| Maximum Operating Voltage | 6.25V |
| DC Output Current | 5.0 mA |

*Notice: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# 3. Block Diagram

**Figure 3-1. Block Diagram**




# 4. Pin Description

**Serial Clock (SCL):** The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

**Serial Data (SDA):** The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

**Device/Page Addresses (A2, A1, and A0):** The A2 and A1 pins are device address inputs that must be hardwired for the AT24HC04B. As many as four 4K devices may be addressed on a single bus system. The A0 pin is a no connect. (Device addressing and Page addressing are discussed in detail in Section 7., “Device Addressing and Page Addressing”).

**Write Protect (WP):** The AT24HC04B has a WP pin which provides hardware data protection. The WP pin allows normal read/write operations when connected to ground (GND). When the WP pin is connected to $V_{CC}$, the write protection feature is enabled and operates as shown.

**Table 4-1. Write Protect**

| WP Pin Status | Part of the Array Protected |
|---|---|
| At $V_{CC}$ | Upper Half (2K) Array |
| At GND | Normal Read/Write Operations |

# 5. Memory Organization

**AT24HC04B, 4K Serial EEPROM:** The 4K is internally organized with 32 pages of 16 bytes each. Random word addressing requires an 9-bit data word address.

## 5.1 Pin Capacitance [1]

Applicable over recommended operating range from $T_{AI}$ = 25°C, f = 1.0MHz, $V_{CC}$ = +1.8V.

| Symbol | Test Condition | Max | Units | Conditions |
|---|---|---|---|---|
| $C_{I/O}$ | Input/Output Capacitance (SDA) | 8 | pF | $V_{I/O}$ = 0V |
| $C_{IN}$ | Input Capacitance ($A_0$, $A_1$, $A_2$, and SCL) | 6 | pF | $V_{IN}$ = 0V |

Note: 1. This parameter is characterized and is not 100% tested.

## 5.2 DC Characteristics

Applicable over recommended operating range from: $T_{AI}$ = -40°C to +85°C, $V_{CC}$ = +1.8V to +5.5V (unless otherwise noted).

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CC1}$ | Supply Voltage | | 1.80 | | 5.50 | V |
| $V_{CC2}$ | Supply Voltage | | 2.50 | | 5.50 | V |
| $V_{CC3}$ | Supply Voltage | | 2.70 | | 5.50 | V |
| $V_{CC4}$ | Supply Voltage | | 4.50 | | 5.50 | V |
| $I_{CC}$ | Supply Current $V_{CC}$ = 5.0V | Read at 100kHz | | 0.40 | 1 | mA |
| $I_{CC}$ | Supply Current $V_{CC}$ = 5.0V | Write at 100kHz | | 2 | 3 | mA |
| $I_{SB1}$ | Standby Current $V_{CC}$ = 1.8V | $V_{IN}$ = $V_{CC}$ or $V_{SS}$ | | 0.60 | 3 | µA |
| $I_{SB2}$ | Standby Current $V_{CC}$ = 2.5V | $V_{IN}$ = $V_{CC}$ or $V_{SS}$ | | 1.40 | 4 | µA |
| $I_{SB3}$ | Standby Current $V_{CC}$ = 2.7V | $V_{IN}$ = $V_{CC}$ or $V_{SS}$ | | 1.60 | 4 | µA |
| $I_{SB4}$ | Standby Current $V_{CC}$ = 5.0V | $V_{IN}$ = $V_{CC}$ or $V_{SS}$ | | 8 | 18 | µA |
| $I_{LI}$ | Input Leakage Current | $V_{IN}$ = $V_{CC}$ or $V_{SS}$ | | 0.10 | 3 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT}$ = $V_{CC}$ or $V_{SS}$ | | 0.05 | 3 | µA |
| $V_{IL}$ | Input Low Level [1] | | –0.60 | | $V_{CC}$ x 0.30 | V |
| $V_{IH}$ | Input High Level [1] | | $V_{CC}$ x 0.70 | | $V_{CC}$ + 0.50 | V |
| $V_{OL2}$ | Output Low Level $V_{CC}$ = 3.0V | $I_{OL}$ = 2.10mA | | | 0.40 | V |
| $V_{OL1}$ | Output Low Level $V_{CC}$ = 1.8V | $I_{OL}$ = 0.15mA | | | 0.20 | V |

Note: 1. $V_{IL}$ min and $V_{IH}$ max are reference only and are not tested.

**Table 5-1. AC Characteristics**

Applicable over recommended operating range from $T_{AI}$ = –40°C to +85°C, $V_{CC}$ = +5.5V, CL = 1 TTL Gate and 100pF (unless otherwise noted). Test conditions are listed in Note 2.

| | | 1.8V, 2.5V, 2.7V | | 5V | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min** | **Max** | **Min** | **Max** | **Units** |
| $f_{SCL}$ | Clock Frequency, SCL | | 400 | | 1000 | kHz |
| $t_{LOW}$ | Clock Pulse Width Low | 1.20 | | 0.40 | | µs |
| $t_{HIGH}$ | Clock Pulse Width High | 0.60 | | 0.40 | | µs |
| $t_I$ | Noise Suppression Time | | 50 | | 40 | ns |
| $t_{AA}$ | Clock Low to Data Out Valid | 0.10 | 0.90 | 0.05 | 0.55 | µs |
| $t_{BUF}$ | Time the bus must be free before a new transmission can start. | 1.20 | | 0.50 | | µs |
| $t_{HD.STA}$ | Start Hold Time | 0.60 | | 0.25 | | µs |
| $t_{SU.STA}$ | Start Setup Time | 0.60 | | 0.25 | | µs |
| $t_{HD.DAT}$ | Data In Hold Time | 0 | | 0 | | µs |
| $t_{SU.DAT}$ | Data In Setup Time | 100 | | 100 | | ns |
| $t_R$ | Inputs Rise Time (1) | | 0.30 | | 0.30 | µs |
| $t_F$ | Inputs Fall Time (1) | | 300 | | 100 | ns |
| $t_{SU.STO}$ | Stop Setup Time | 0.60 | | .25 | | µs |
| $t_{DH}$ | Data Out Hold Time | 50 | | 50 | | ns |
| $t_{WR}$ | Write Cycle Time | | 5 | | 5 | ms |
| Endurance(1) | 5.0V, 25°C, Byte Mode | 1,000,000 | | | | Write Cycles |

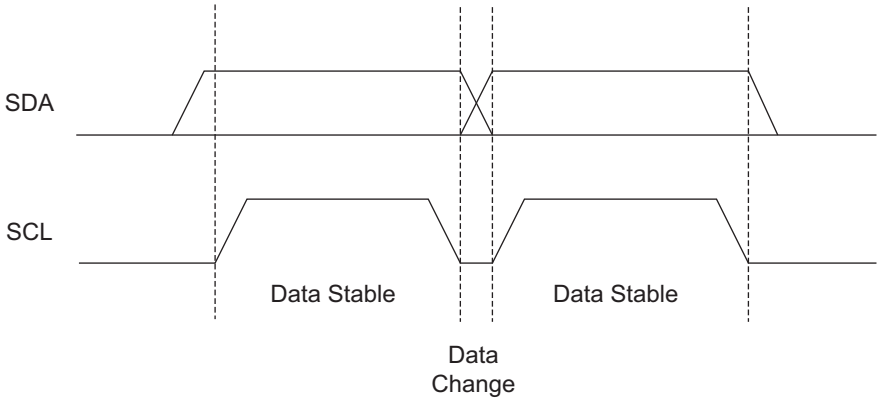
Notes: 1. This parameter is ensured by characterization only.

2. AC measurement conditions:
   - RL (connects to $V_{CC}$): 1.3kΩ (2.5V, 5.5V), 10kΩ (1.7V)
   - Input pulse voltages: $0.3V_{CC}$ to $0.7V_{CC}$
   - Input rise and fall times: ≤ 50ns
   - Input and output timing reference voltages: 0.5 x $V_{CC}$

# 6. Device Operation

**Clock and Data Transitions:** The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods will indicate a Start or Stop condition as defined below.

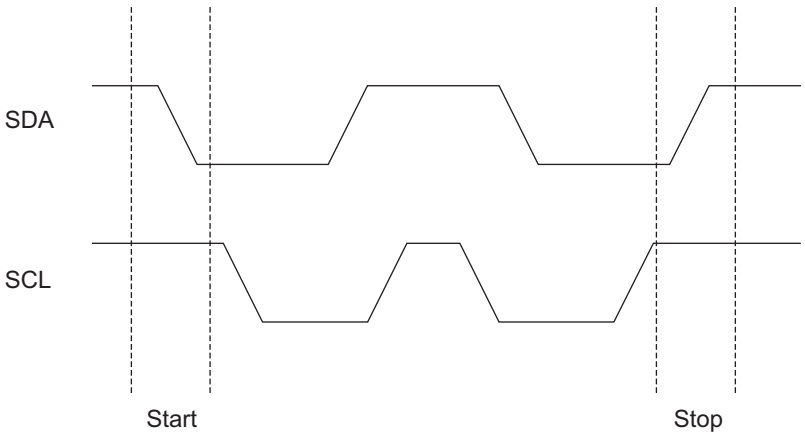
**Figure 6-1. Data Validity**




**Start Condition:** A high-to-low transition of SDA with SCL high is a Start condition that must precede any other command.

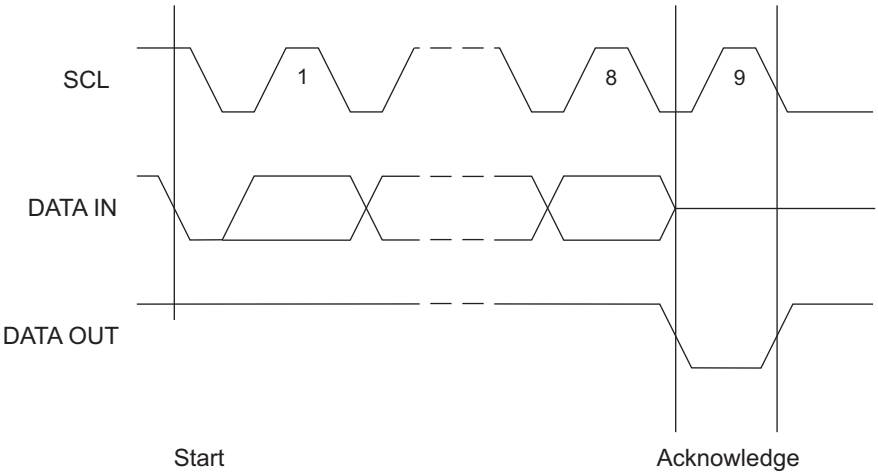
**Stop Condition:** A low-to-high transition of SDA with SCL high is a Stop condition. After a read sequence, the Stop condition will place the EEPROM in a standby power mode.

**Figure 6-2. Start and Stop Definition**



**Acknowledge:** All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

**Figure 6-3. Output Acknowledge**




**Standby Mode:** The AT24HC04B features a low-power standby mode that is enabled:

- Upon power-up.
- After the receipt of the Stop condition, and the completion of any internal operations.

**2-Wire Software Reset:** After an interruption in protocol, power loss or system reset, any 2-wire part can be protocol reset by following these steps:

1. Create a start condition (if possible).
2. Clock nine cycles.
3. Create another Start condition followed by Stop condition as shown below.

The device should be ready for the next communication after above steps have been completed. In the event that the device is still non-responsive or remains active on the SDA bus, a power cycle must be used to reset the device.

**Figure 6-4. Software Reset**

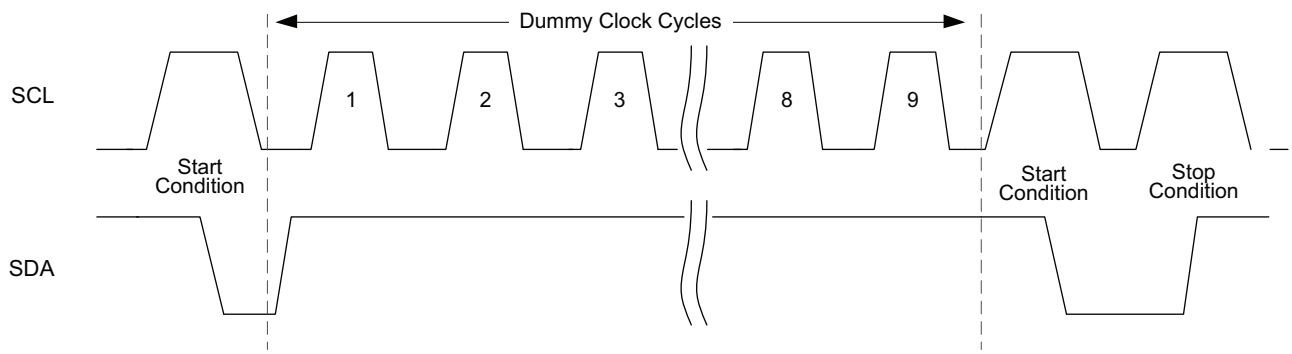


**Figure 6-5. Bus Timing**

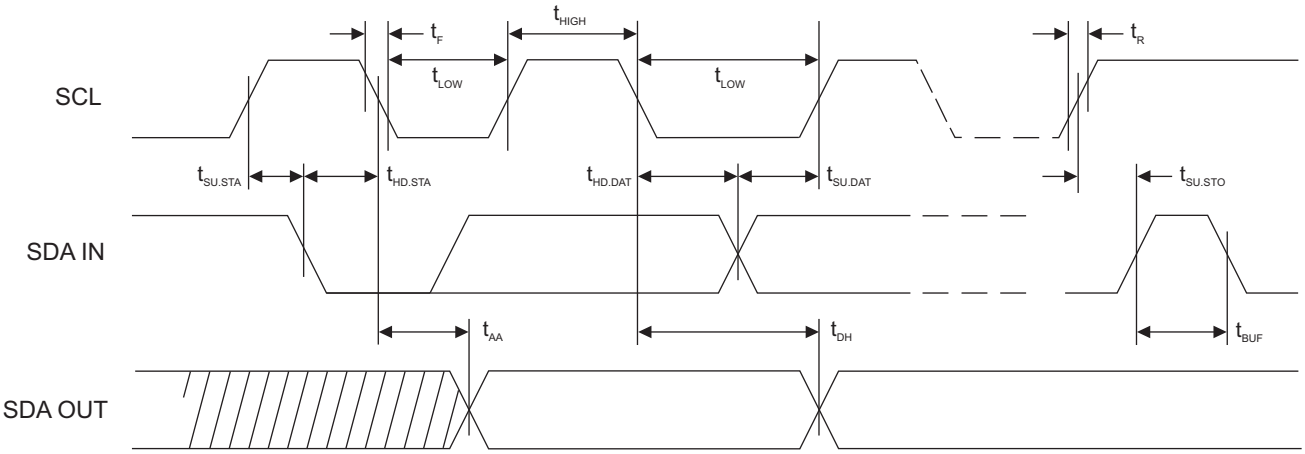
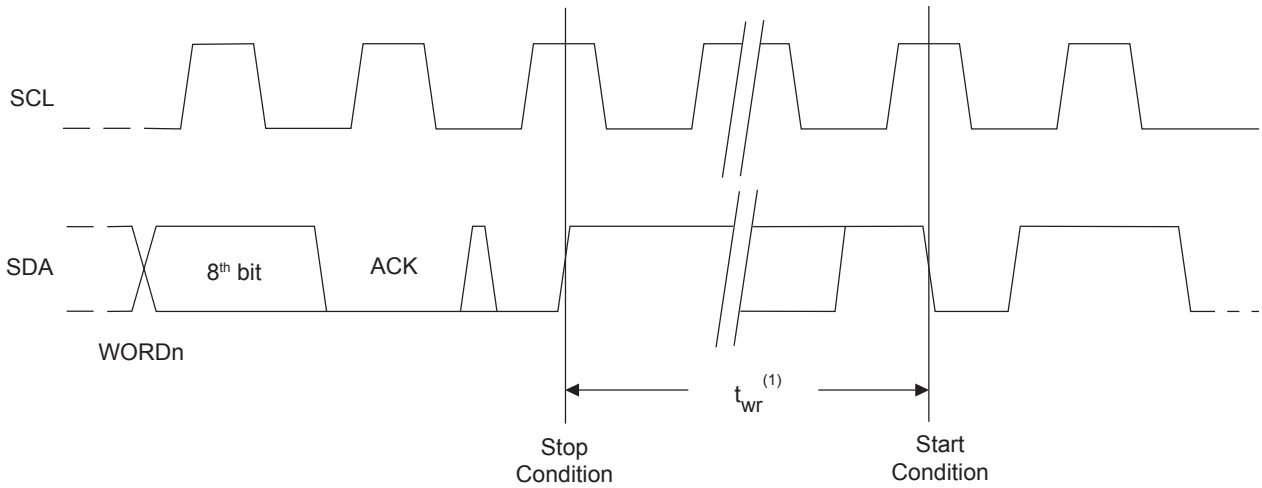



**Figure 6-6. Write Cycle Timing**

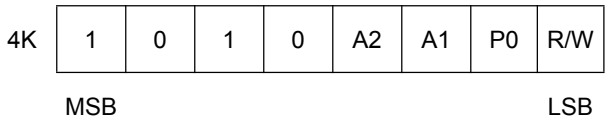



Note: 1. The write cycle time $t_{WR}$ is the time from a valid Stop condition of a write sequence to the end of the internal clear/write cycle.

# 7. Device Addressing and Page Addressing

The 4K EEPROM device requires an 8-bit device address word following a Start condition to enable the chip for a read or write operation, as shown in the below figure.

**Figure 7-1. Device Address**




The device address word consists of a mandatory “1”, “0” sequence for the first four most significant bits as shown. This is common to all the EEPROM devices.

The next two bits are the A2 and A1 device address bits for the 4K EEPROM. These two bits must compare to their corresponding hardwired input pins. The A0 pin is a no connect.

The next bit is the memory page address bit. This bit is the MSB of the 9-bit data word address.

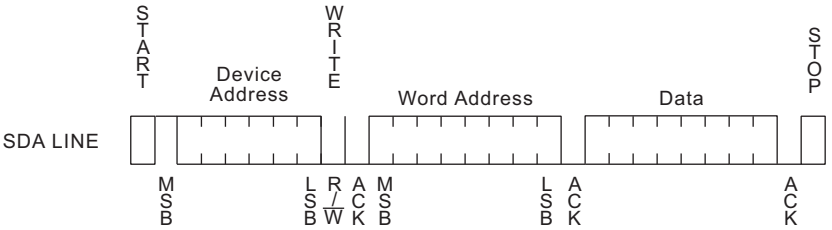
The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high, and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the chip will return to a standby state.

# 8. Write Operations

**Byte Write:** A Write operation requires an 8-bit data word address following the device address word and acknowledgement. Upon receipt of this address, the EEPROM will again respond with a zero, and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero and the addressing device, such as a microcontroller, must terminate the write sequence with a Stop condition. At this time, the EEPROM enters an internally-timed write cycle, $t_{WR}$, to the nonvolatile memory. All inputs are disabled during this write cycle, and the EEPROM will not respond until the write is complete.

**Figure 8-1. Byte Write**

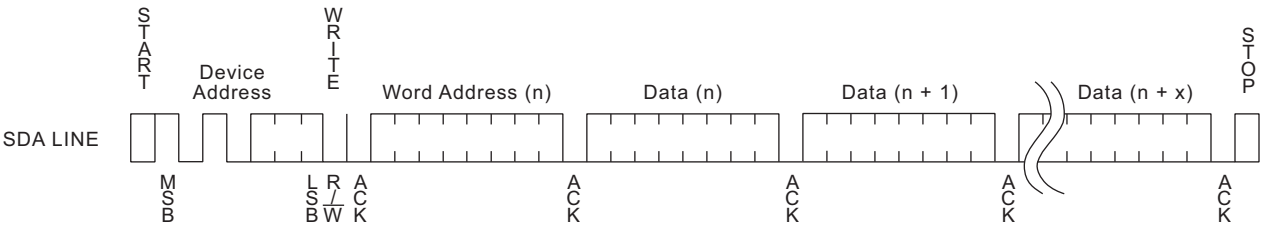



**Page Write:** The 4K EEPROM is capable of a 16-byte Page Write.

A Page Write is initiated the same as a Byte Write, but the microcontroller does not send a Stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to fifteen more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the Page Write sequence with a Stop condition.

The data word address lower four bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than sixteen data words are transmitted to the EEPROM, the data word address will roll-over and previous data will be overwritten.

**Figure 8-2. Page Write**




**Acknowledge Polling:** Once the internally-timed write cycle has started and the EEPROM inputs are disabled, Acknowledge Polling can be initiated. This involves sending a Start condition followed by the device address word. The Read/Write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero allowing the read or write sequence to continue.

# 9. Read Operations

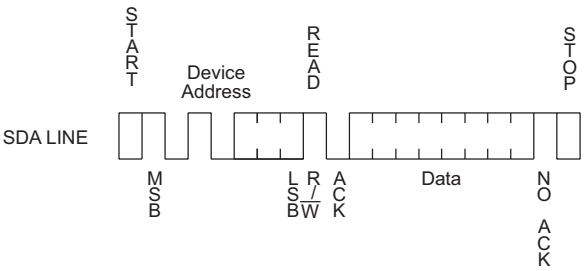
Read operations are initiated the same way as Write operations with the exception that the Read/Write select bit in the device address word is set to one. There are three Read operations:

- Current Address Read
- Random Address Read
- Sequential Read

**Current Address Read:** The internal data word address counter maintains the last address accessed during the last Read or Write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address roll-over during read is from the last byte of the last memory page to the first byte of the first page. The address roll-over during write is from the last byte of the current page to the first byte of the same page.

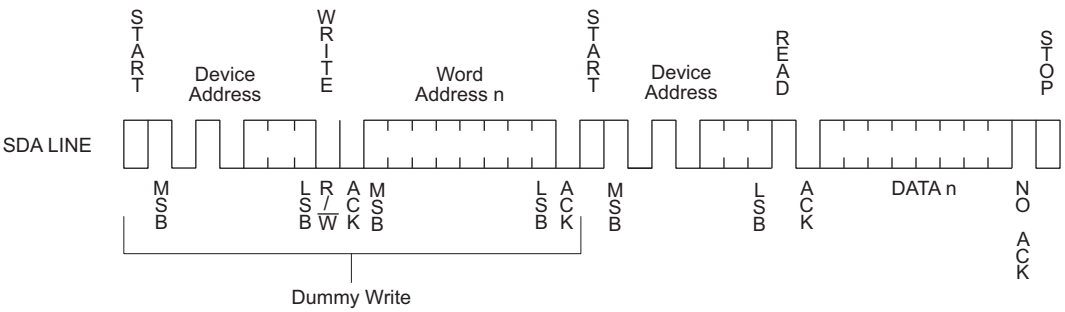
Once the device address with the Read/Write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a following Stop condition.

**Figure 9-1. Current Address Read**



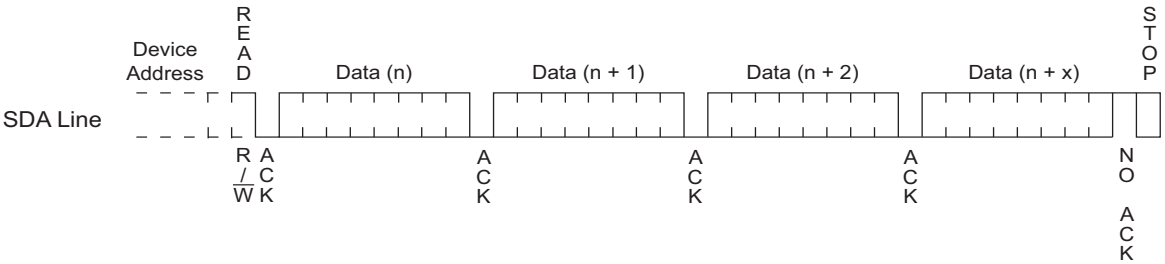

**Random Read:** A Random Read requires a dummy byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another Start condition. The microcontroller now initiates a Current Address Read by sending a device address with the Read/Write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a following Stop condition.

**Figure 9-2. Random Read**

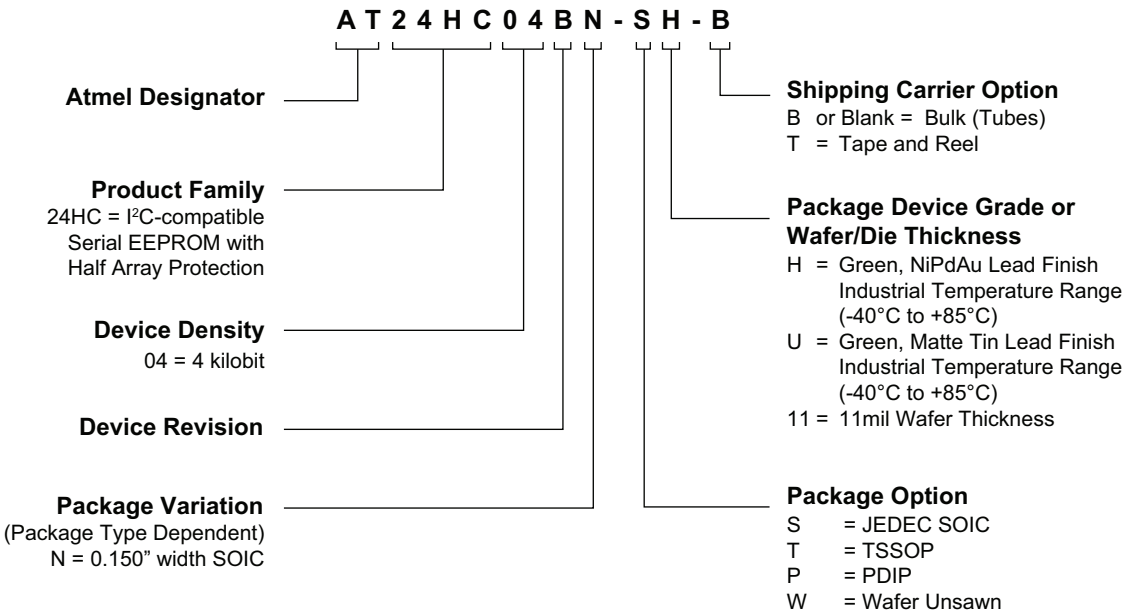


**Sequential Read:** Sequential Reads are initiated by either a current address read or a Random Address Read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an Acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll-over and the Sequential Read will continue. The Sequential Read operation is terminated when the microcontroller does not respond with a zero but does generate a following Stop condition.

**Figure 9-3. Sequential Read**



## 10. Ordering Code Detail




## 11. Ordering Code Information

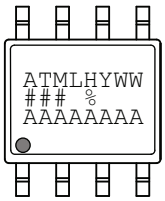
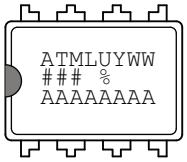
| Atmel Ordering Code | Lead Finish | Package | Voltage | Delivery Information | | Operation Range |
|---|---|---|---|---|---|---|
| | | | | Form | Quantity | |
| AT24HC04B-PU | Matte Tin (Lead-free/Halogen-free) | 8P3 | 1.8V | Bulk (Tubes) | 50 per Tube | Industrial Temperature (-40°C to 85°C) |
| AT24HC04BN-SH-B | NiPdAu (Lead-free/Halogen-free) | 8S1 | | Bulk (Tubes) | 100 per Tube | |
| AT24HC04BN-SH-T | | | | Tape and Reel | 4,000 per Reel | |
| AT24HC04B-TH-B | | 8X | | Bulk (Tubes) | 100 per Tube | |
| AT24HC04B-TH-T | | | | Tape and Reel | 5,000 per Reel | |
| AT24HC04B-W-11 | N/A | Wafer Sale | | Note 1 | | |

Note: 1. Available in tape and reel and wafer form; order as SL788 for inkless wafer form. Bumped die available upon request. Please contact the Atmel sales office.

| Package Type | |
|---|---|
| **8P3** | 8-pin, 0.30" wide, Plastic Dual Inline (PDIP) |
| **8S1** | 8-lead, 0.15" wide, Plastic Gull Wing Small Outline (JEDEC SOIC) |
| **8X** | 8-lead, 4.40mm body, Plastic Thin Shrink Small Outline (TSSOP) |

# 12. Part Marking Scheme

## AT24HC04B Package Marking Information

| 8-lead SOIC | 8-lead TSSOP | 8-lead PDIP |
|---|---|---|
|  |  |  |





*Note: Lot Number and location of assembly and on the bottom side of the package.*



Note 1: ● designates pin 1
Note 2: Package drawings are not to scale

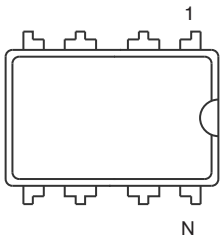
| **Catalog Number Truncation** | | | |
|---|---|---|---|
| AT24HC04B | | Truncation Code ###: H4B | |
| **Date Codes** | | | **Voltages** |
| Y = Year | M = Month | WW = Work Week of Assembly | % = Minimum Voltage |
| 4: 2014 8: 2018<br>5: 2015 9: 2019<br>6: 2016 0: 2020<br>7: 2017 1: 2021 | A: January<br>B: February<br>...<br>L: December | 02: Week 2<br>04: Week 4<br>...<br>52: Week 52 | 1: 1.8V min |
| **Country of Assembly** | **Lot Number** | | **Grade/Lead Finish Material** |
| @ = Country of Assembly | AAA...A = Atmel Wafer Lot Number | | U: Industrial/Matte Tin/SnAgCu<br>H: Industrial/NiPdAu |
| **Trace Code** | | | **Atmel Truncation** |
| XX = Trace Code (Atmel Lot Numbers Correspond to Code)<br>Example: AA, AB.... YZ, ZZ | | | AT: Atmel<br>ATM: Atmel<br>ATML: Atmel |

6/10/15

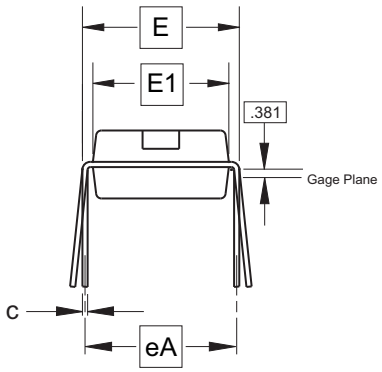
| Atmel<br>Package Mark Contact:<br>DL-CSO-Assy_eng@atmel.com | **TITLE**<br>**24HC04BSM**, AT24HC04B Package Marking Information | **DRAWING NO.**<br>24HC04BSM | **REV.**<br>B |
|---|---|---|---|

# 13. Packaging Information

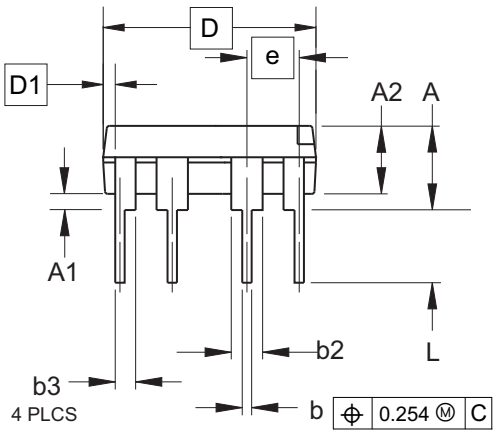
## 13.1 8P3 — 8-lead PDIP




Top View




End View




Side View

COMMON DIMENSIONS
(Unit of Measure = mm)

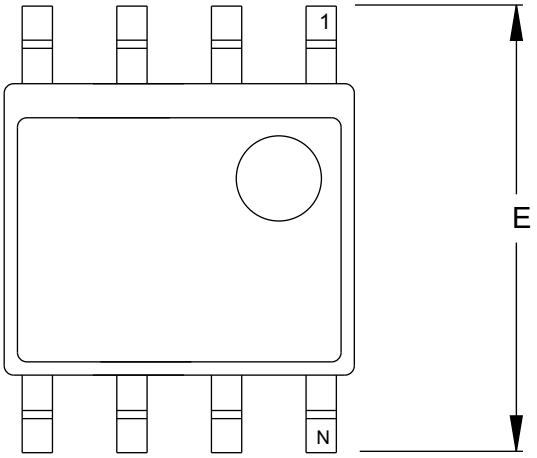
| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | - | - | 5.334 | 2 |
| A1 | 0.381 | - | - | |
| A2 | 2.921 | 3.302 | 4.953 | |
| b | 0.356 | 0.457 | 0.559 | 5 |
| b2 | 1.143 | 1.524 | 1.778 | 6 |
| b3 | 0.762 | 0.991 | 1.143 | 6 |
| c | 0.203 | 0.254 | 0.356 | |
| D | 9.017 | 9.271 | 10.160 | 3 |
| D1 | 0.127 | 0.000 | 0.000 | 3 |
| E | 7.620 | 7.874 | 8.255 | 4 |
| E1 | 6.096 | 6.350 | 7.112 | 3 |
| e | 2.540 BSC | | | |
| eA | 7.620 BSC | | | 4 |
| L | 2.921 | 3.302 | 3.810 | 2 |

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA for additional information.
2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
4. E and eA measured with the leads constrained to be perpendicular to datum.
5. Pointed or rounded lead tips are preferred to ease insertion.
6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

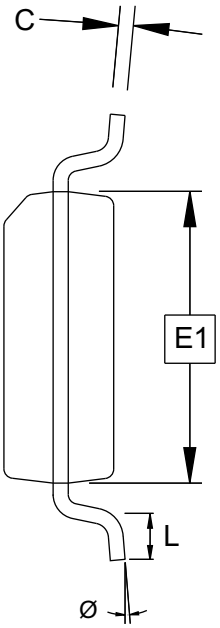
07/31/14

| Atmel<br>Package Drawing Contact:<br>packagedrawings@atmel.com | TITLE<br>8P3, 8-lead, 0.300” Wide Body, Plastic Dual In-line Package (PDIP) | GPC<br>PTC | DRAWING NO.<br>8P3 | REV.<br>E |
|---|---|---|---|---|

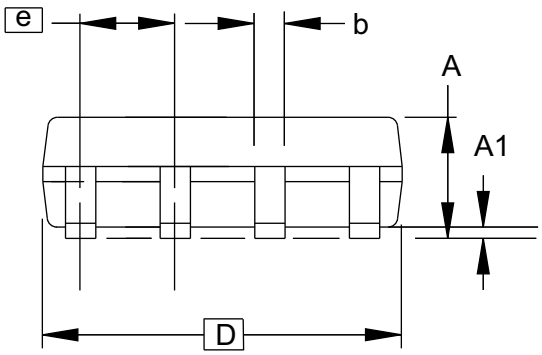
## 13.2 8S1 — 8-lead JEDEC SOIC




TOP VIEW




END VIEW




SIDE VIEW

Notes: This drawing is for general information only.
Refer to JEDEC Drawing MS-012, Variation AA
for proper dimensions, tolerances, datums, etc.

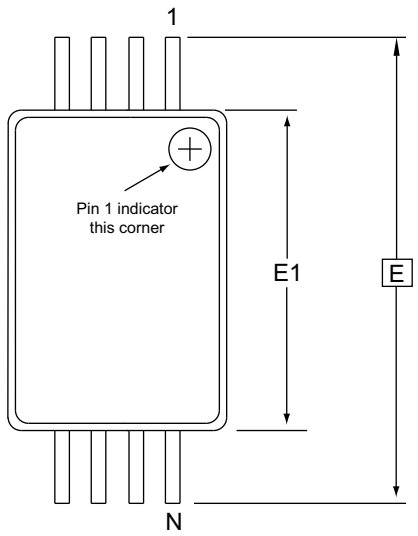
COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | – | – | 1.75 | |
| A1 | 0.10 | – | 0.25 | |
| b | 0.31 | – | 0.51 | |
| C | 0.17 | – | 0.25 | |
| D | | 4.90 BSC | | |
| E | | 6.00 BSC | | |
| E1 | | 3.90 BSC | | |
| e | | 1.27 BSC | | |
| L | 0.40 | – | 1.27 | |
| Ø | 0° | – | 8° | |

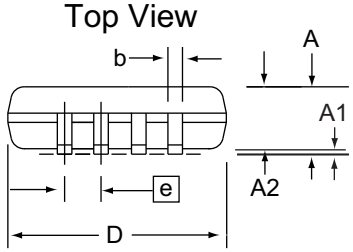
3/6/2015

| Atmel<br>Package Drawing Contact:<br>packagedrawings@atmel.com | **TITLE**<br>8S1, 8-lead (0.150” Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC) | **GPC**<br>SWB | **DRAWING NO.**<br>8S1 | **REV.**<br>H |
|---|---|---|---|---|

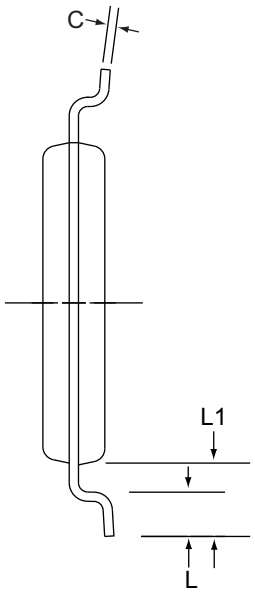
## 13.3 8X — 8-lead TSSOP




Top View




Side View




End View

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15mm (0.006in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
5. Dimension D and E1 to be determined at Datum Plane H.

COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | - | - | 1.20 | |
| A1 | 0.05 | - | 0.15 | |
| A2 | 0.80 | 1.00 | 1.05 | |
| D | 2.90 | 3.00 | 3.10 | 2, 5 |
| E | | 6.40 BSC | | |
| E1 | 4.30 | 4.40 | 4.50 | 3, 5 |
| b | 0.19 | 0.25 | 0.30 | 4 |
| e | | 0.65 BSC | | |
| L | 0.45 | 0.60 | 0.75 | |
| L1 | | 1.00 REF | | |
| C | 0.09 | - | 0.20 | |

2/27/14

| Atmel<br>Package Drawing Contact:<br>packagedrawings@atmel.com | TITLE<br>8X, 8-lead 4.4mm Body, Plastic Thin Shrink Small Outline Package (TSSOP) | GPC<br>TNR | DRAWING NO.<br>8X | REV.<br>E |
|---|---|---|---|---|

# 14. Revision History

| Doc. Rev. | Date | Comments |
|---|---|---|
| 5227H | 12/2015 | Corrected the ordering code detail. |
| 5227G | 06/2015 | Updated package drawings, ordering code table, and part marking page.<br>Added the ordering code detail. |
| 5227F | 02/2014 | Updated Atmel template (no changes to functional specification). logos, and disclaimer page, part markings to a single page, and package drawings 8P3, 8S1, and 8A2 to 8X.<br>Updated the Random Read figure and add the AC measurement conditions note to the AC Characteristics table. |
| 5227E | 11/2008 | Updated pin configurations. |
| 5227D | 01/2008 | Removed ‘preliminary’ status. |
| 5227C | 08/2007 | Added Part Marking Scheme. |
| 5227B | 08/2007 | Updated to new template and common figures.<br>Added Part Marking tables. |
| 5227A | 04/2007 | Initial document release. |

Atmel | Enabling Unlimited Possibilities®

**Atmel Corporation** 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441.0311 **F:** (+1)(408) 436.4200 | **www.atmel.com**