MP2014

40V, 500mA, Low Quiescent Current Linear Regulator

The Future of Analog IC Technology

DESCRIPTION

The MP2014 is a low power linear regulator that supplies power to systems with high voltage batteries. It includes a wide 3V to 40V input range, low dropout voltage and low quiescent supply current. The low quiescent current and low dropout voltage allow operations at extremely low power levels. Therefore, the MP2014 is ideal for the low power microcontrollers and the battery-powered equipments.

The MP2014 provides wide variety of fixed output voltage options (if request): 1.8V, 1.9V, 2.3V, 2.5V, 3.0V, 3.3V, 3.45V, 5.0V.

The regulator output current is internally limited and the device is protected against short-circuit, over-load and over-temperature conditions.

The MP2014 also includes thermal shutdown and current limiting fault protection, and is available in TO252-5 package.

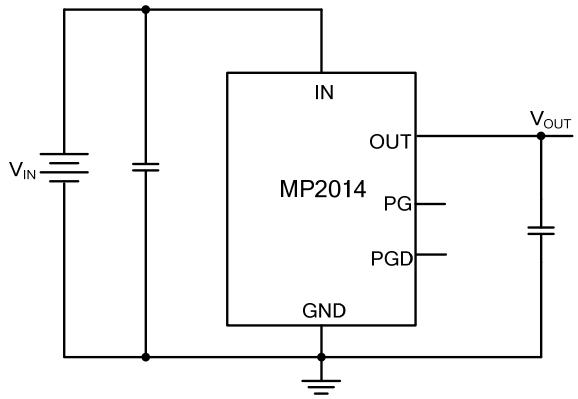
FEATURES

- 3V to 40V Input Range
- 10μA Quiescent Supply Current
- Stable with Low-Value Output Ceramic Capacitor (>0.47μF)
- 500mA Specified Current
- Fixed Output Voltage
- Output ±2% Accuracy
- Specified Current Limit
- Power Good
- Programmable Power Good Delay
- Thermal Shutdown and Short-Circuit Protection
- -40°C to +150°C Specified Junction Temperature Range
- Available in TO252-5 Package

APPLICATIONS

- Industrial/Automotive Applications
- Portable/Battery-Powered Equipment
- Ultra Low Power Microcontrollers
- Cellular Handsets
- Medical Imaging

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2014GZD	TO252-5	*See Below*
MP2014GZD-33	TO252-5	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP2014GZD–Z)

TOP MARKING (MP2014GZD)

MPSYYWW
MP2014
LLLLLLLLL

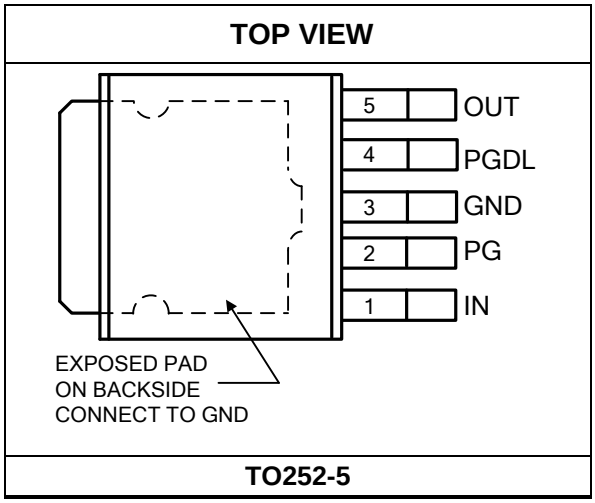
MPS: MPS Prefix
YY: Year Code
WW: Week Code
MP2014: Product Code of MP2014GZD
LLLLLLLLL: Lot Number

TOP MARKING (MP2014GZD-33)

MPS YYWW
MP2014-33
LLLLLLLLL

MPS: MPS Prefix
YY: Year Code
WW: Week Code
MP2014-33: Product Code of MP2014GZD-33
LLLLLLLLL: Lot Number

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

IN .....-0.3V to +42V
OUT .....-0.3V to +17V
PG .....-0.3V to +15V
PGDL .....-0.3V to +6V
Lead Temperature .....260°C
Storage Temperature..... -65°C to +150°C
Continuous Power Dissipation (T_A = +25°C) (2)
TO252-5..... 2.27W

ESD SUSCEPTIBILITY (3)

HBM (Human Body Mode) 4kV
MM (Machine Mode) 200V

Recommended Operating Conditions (4)

Supply Voltage V_{IN} .....3V to 40V
Operating Temperature ..... T_A=-40°C to +125°C
$T_A \leq T_J \leq$ +150°C

Thermal Resistance (5)

	θ_{JA}	θ_{JC}	
TO252-5	55	3	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Devices are ESD sensitive. Handling precaution recommended.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} =13.5V, T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
GND Pin Current	I_{GND}	0<I_{OUT}<1mA		12	17	µA
		1mA<I_{OUT}<30mA		16	22	
		30mA<I_{OUT}<500mA		105	150	
Load Current Limit	I_{LIMIT}	V_{OUT} = 0V	550	900	1450	mA
Output Voltage accuracy		MP2014GZD, V_{IN} =6V to 40V, I_{LOAD} = 5mA	4.9	5	5.1	V
		MP2014GZD-33, V_{IN} =4.3V to 40V, I_{LOAD} = 5mA	3.234	3.3	3.366	
Dropout Voltage[6]	$V_{DROPOUT}$	MP2014GZD, I_{LOAD} = 300mA, $V_{DROPOUT}$=V_{IN}-V_O		400	650	mV
		MP2014GZD-33, I_{LOAD} = 300mA, $V_{DROPOUT}$=V_{IN}-V_O		500	700	
		MP2014GZD, I_{LOAD} = 500mA, $V_{DROPOUT}$=V_{IN}-V_O		750	1000	
		MP2014GZD-33, I_{LOAD} = 500mA, $V_{DROPOUT}$=V_{IN}-V_O		1000	1300	
Line Regulation		V_{IN} = 8V to 40V, I_{LOAD} = 5mA	-10	1	10	mV
Load Regulation		I_{LOAD} = 5mA to 500mA		1	15	mV
Output Voltage PSRR[7]		100Hz, C_{OUT} = 10µF, I_{LOAD}=10mA		57		dB
		1kHz, C_{OUT} = 10µF, I_{LOAD}=10mA		45		dB
		100kHz, C_{OUT} = 10µF, I_{LOAD}=10mA		51		dB
Startup Response Time		MP2014GZD, I_{LOAD}=10mA, C_{OUT}=22µF		1	2	ms
		MP2014GZD-33, I_{LOAD}=10mA, C_{OUT}=22µF		0.6	1.5	
PG Rising Threshold			90%	93%	96%	V_{OUT}
PG Rising Threshold Hysteresis				5%		V_{OUT}
PG Low Voltage		Sink 1mA current		0.1	0.4	V
PG Leakage Current		V_{PG}=5V			1	µA
PGDL Charging Current	I_{PGDL}	V_{PGDL}=1V	3	5.5	9	µA
PGDL Rising Threshold			1.5	1.65	2	V
PGDL Falling Threshold			0.2	0.4	0.7	V
PG Delay Time	t_{PGDL}	C_{PGDL}=47nF, 10% to 90% PGDL Rising Threshold	6	11	14	ms
PG Reaction Time		C_{PGDL}=47nF		0.5	2	µs
Thermal Shutdown[7]	T_{SD}			165		°C
Thermal Shutdown Hysteresis[7]	ΔTSD			30		°C

Notes:

6) Dropout voltage: Measured when the output voltage V_{OUT} has dropped 100mV from the nominal value obtained at V_{IN}=13.5V.

7) Derived from bench characterization. Not tested in production.

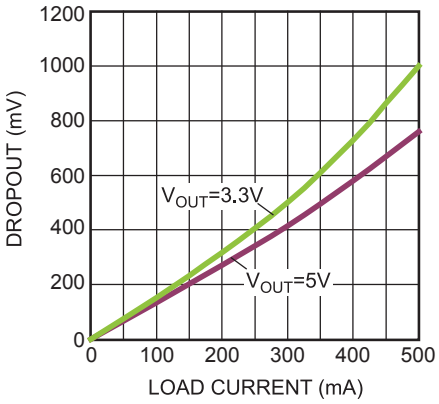
PIN FUNCTIONS

Pin #	Name	Description
1	IN	Input voltage. Connect a 3V to 40V supply to this pin.
2	PG	Power good.
3	GND	Ground (internally connected to the exposed pad, GND pin and the exposed pad must be connected to the same ground plane)
4	PGDL	Programmable power good delay time.
5	OUT	Regulated output voltage, only low-value ceramic capacitor (≥0.47μF) on output is required for stability.

TYPICAL PERFORMANCE CHARACTERISTICS

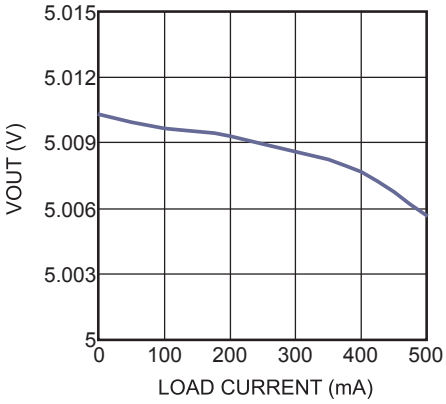
C_{IN} = 1µF, C_{OUT} = 22µF, V_{OUT} = 5V, T_A = 25°C, unless otherwise noted.

Dropout vs. Load Current



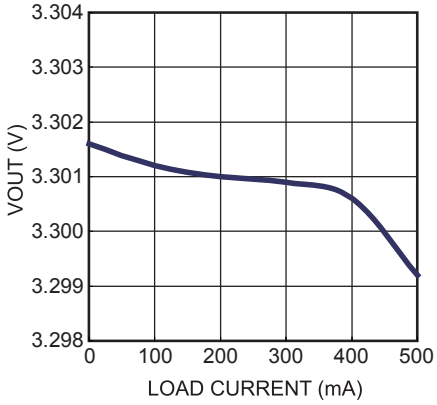
VOUT vs. IOUT

MP2014GZD, V_{IN}=6V



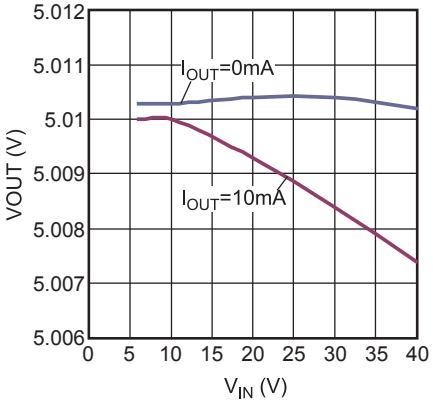
VOUT vs. IOUT

MP2014GZD-33, V_{IN}=4.5V



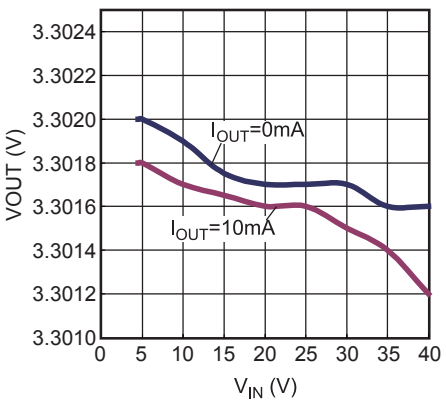
VOUT vs. VIN

MP2014GZD



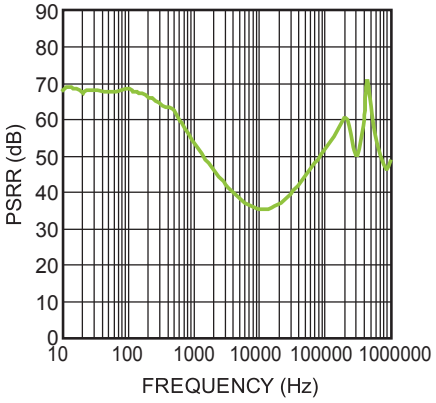
VOUT vs. VIN

MP2014GZD-33



PSRR vs. Frequency

C_{IN}=100pF, C_{OUT}=10µF, I_{OUT}=10mA

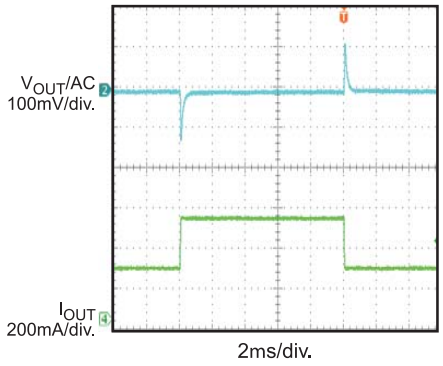


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

C_{IN} = 1µF, C_{OUT} = 22µF, V_{OUT} = 5V, T_A = 25°C, unless otherwise noted.

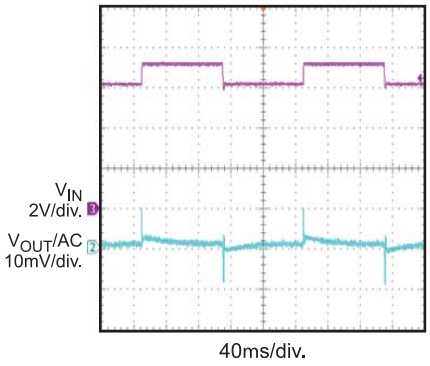
Load Transient

V_{IN}=12V, I_{OUT}=250mA-500mA



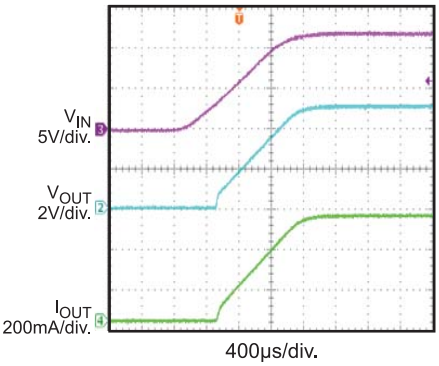
Line Transient

V_{IN}=6V-7V, I_{OUT}=500mA



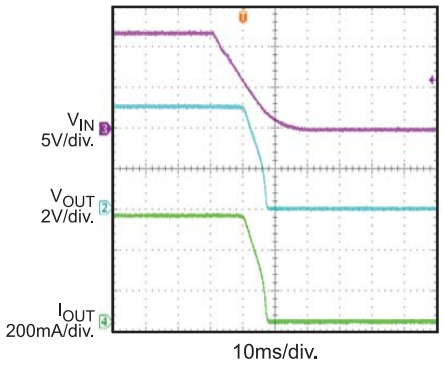
Start-Up through V_{IN}

V_{IN}=12V, I_{OUT}=500mA



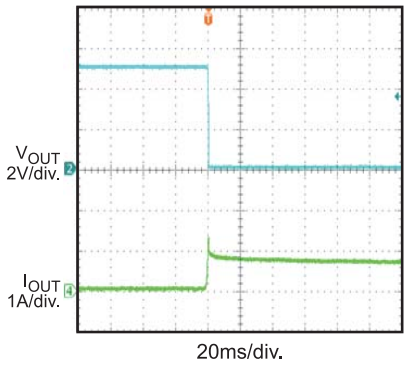
Shutdown through V_{IN}

V_{IN}=12V, I_{OUT}=500mA



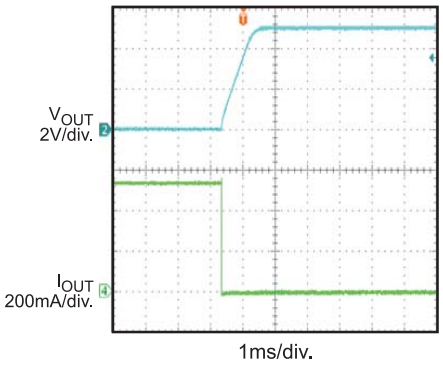
Short-Circuit Entry

I_{OUT}=0mA to Short Circuit



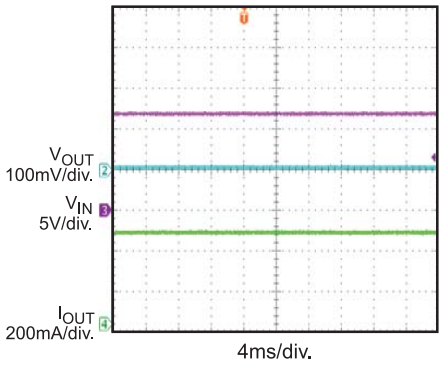
Short-Circuit Recovery

Short Circuit to I_{OUT}=0mA



Short-Circuit Steady State

V_{IN}=12V



OPERATION

The MP2014 is a linear regulator that supplies power to systems with high voltage batteries. It includes a wide 3V to 40V input range, low dropout voltage and low quiescent supply current.

The MP2014 provides wide variety of fixed output voltage options: 1.8V, 1.9V, 2.3V, 2.5V, 3.0V, 3.3V, 3.45V, 5.0V.

Short-Circuit Protection

The regulator output current is internally limited and the device is protected against short-circuit, over-load. The peak output current is limited to around 900mA, which exceeds the 500mA recommended continuous output current.

Thermal Shutdown

When the junction temperature exceeds the upper threshold (165°C), the thermal sensor sends a signal to the control logic to shutdown the IC. The IC will restart when the temperature has sufficiently cooled (135°C).

The maximum power output current is a function of the package's maximum power dissipation for a given temperature.

The maximum power dissipation is dependent on the thermal resistance of the case and the circuit board, the temperature difference between the die junction and the ambient air, and the rate of air flow. The GND pin and Exposed Pad must be connected to the ground plane for proper dissipation.

Power Good Output

MP2014 has one power good (PG) pin. The PG pin is the open drain of an internal MOSFET. It should be connected to V_{OUT} or external voltage source(<15V) through a resistor (i.e. 100kohm). After the V_{OUT} reaches 93% of nominal value, the MOSFET turns off and PG pin is pulled to high by V_{OUT} or external voltage source. When the V_{OUT} drops to 88% of nominal value, the PG voltage is pulled to GND.

There is a delay time when PG asserts high. The delay time can be programmed by adding a capacitor on PGDL. To select a capacitor for PGDL, use below equation:

$$C_{PGDL}(nF) = \frac{t_{PGDL}(ms) \times I_{PGDL}(\mu A)}{V_{th\_PGDL}(V)}$$

Where t_{PGDL} is the desired delay time for PG asserts high, I_{PGDL} is the PGDL charging current and V_{th_PGDL} is 1.65V.

Figure 2 shows the power good timing.

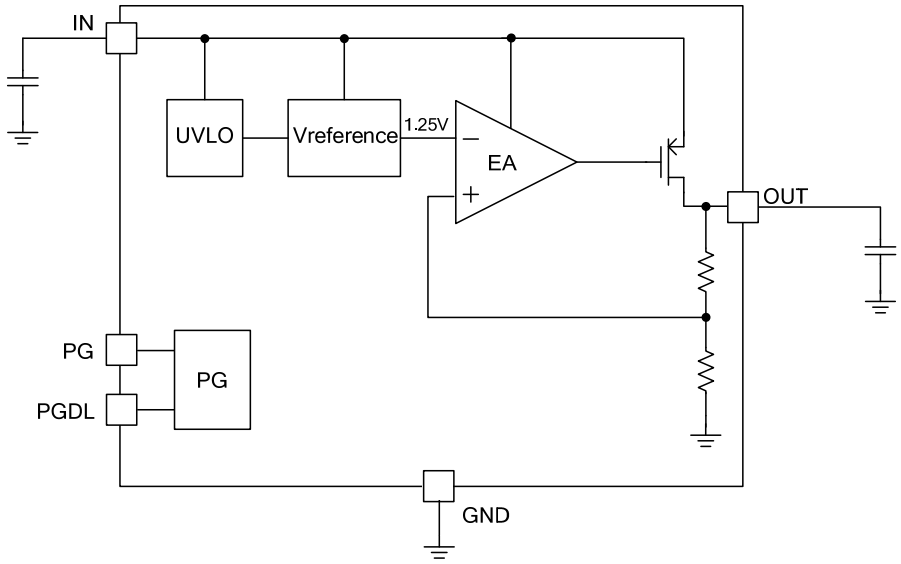


Figure 1: Functional Block Diagram

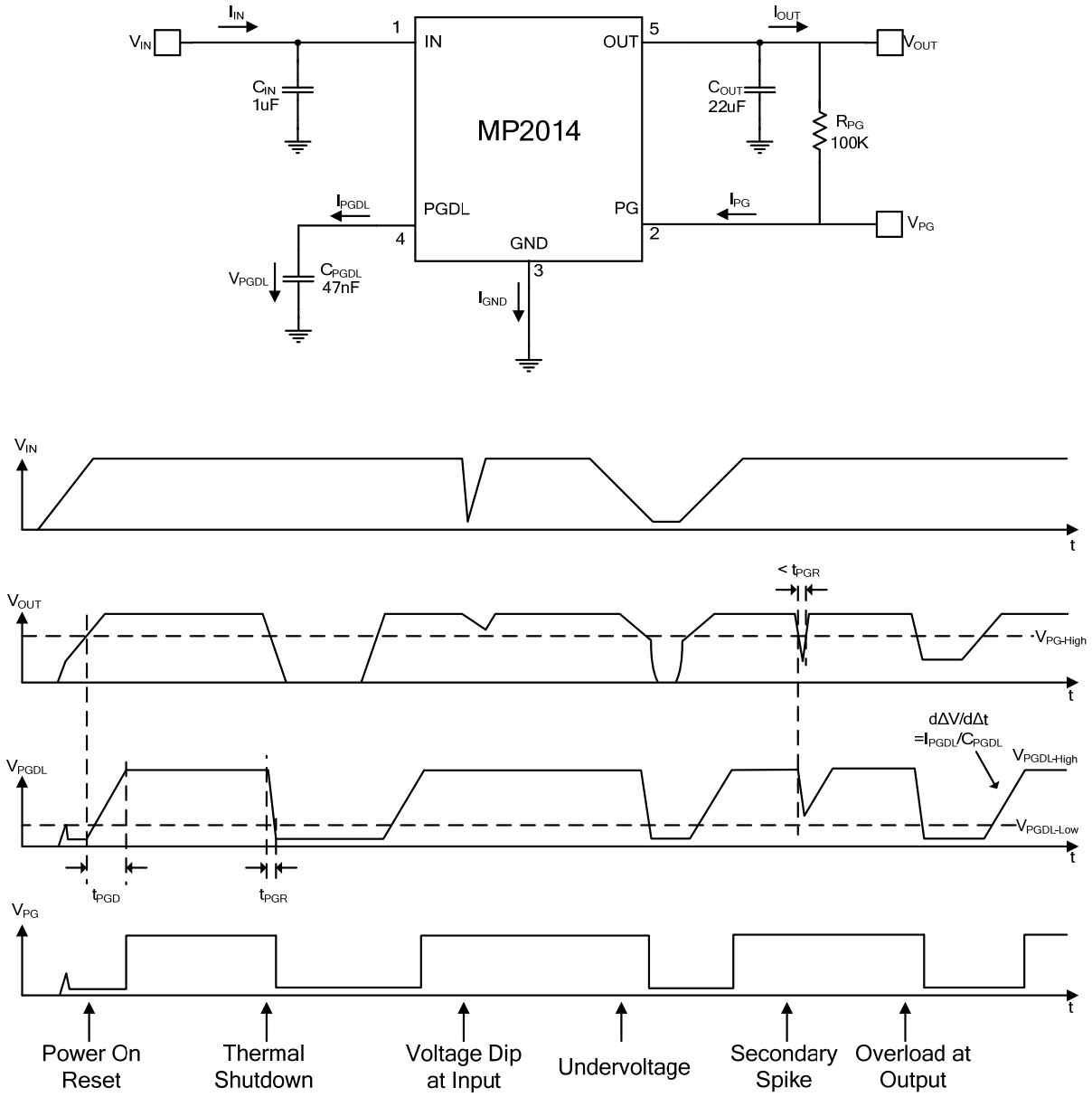


Figure 2: Power Good Timing

APPLICATION INFORMATION

Component Selection

Input Capacitor

For proper operation, place a ceramic capacitor (C1) between 1μF and 10μF of dielectric type X5R or X7R between the input pin and ground. Larger values in this range will help improve line transient response.

Output Capacitor

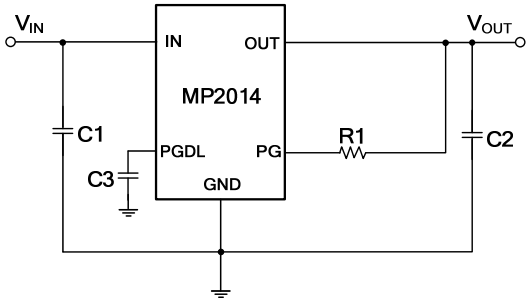
For stable operation, use a ceramic capacitor (C2) of type X5R or X7R between 1μF and 22μF. Larger values in this range will help improve load transient response and reduce noise. Output capacitors of other dielectric types may be used, but are not recommended as their capacitance can deviate greatly from their rated value over temperature.

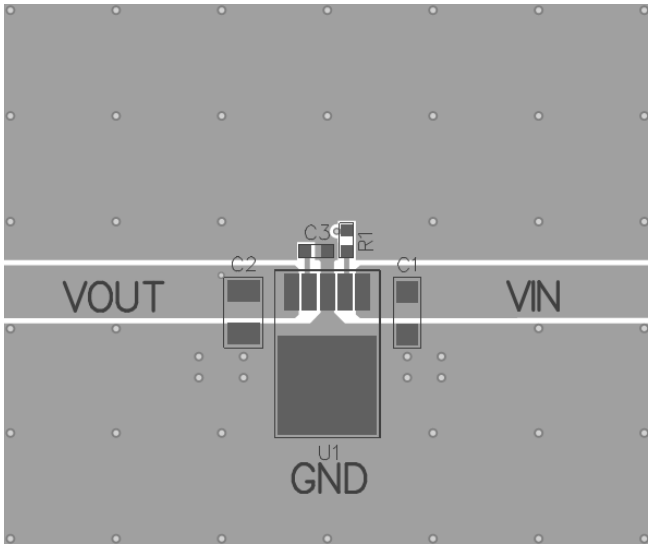
PCB Layout Guide

PCB layout is very important to achieve good regulation, ripple rejection, transient response and thermal performance. It is highly recommended to duplicate EVB layout for optimum performance.

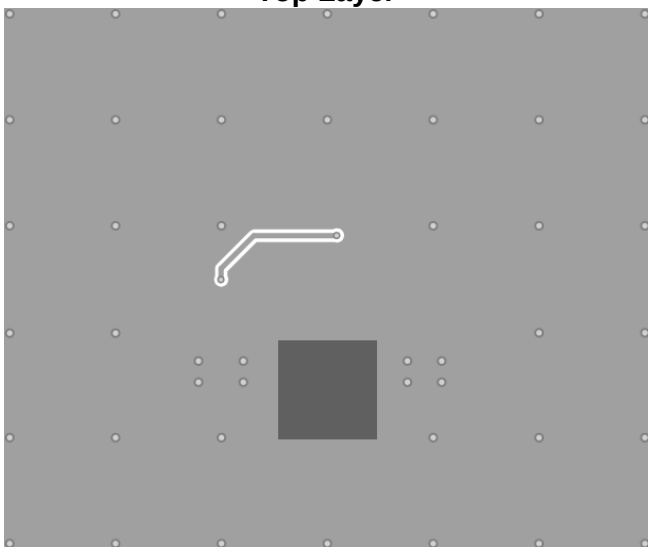
If change is necessary, please follow these guidelines and take figure 3 for reference.

1) Input and output bypass ceramic capacitors are suggested to be put close to the IN Pin and OUT Pin respectively.
2) Connect IN, OUT and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.





Top Layer



Bottom Layer

Figure 3: PCB Layout

DESIGN EXAMPLE

Below is a design example following the application guidelines.

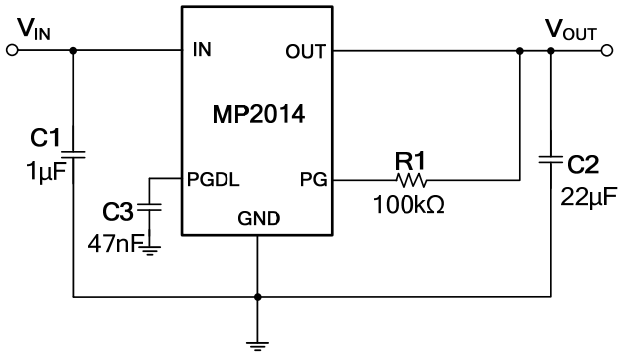


Figure 4: Design Example

TYPICAL APPLICATION CIRCUITS

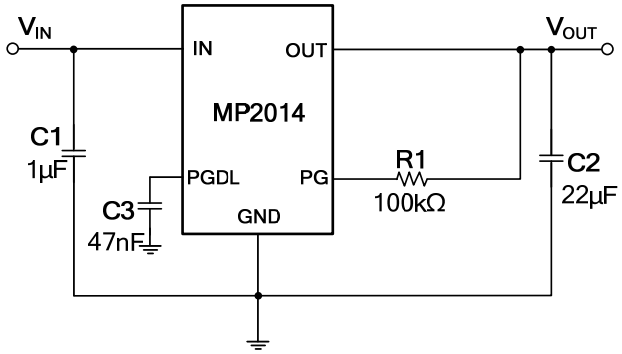
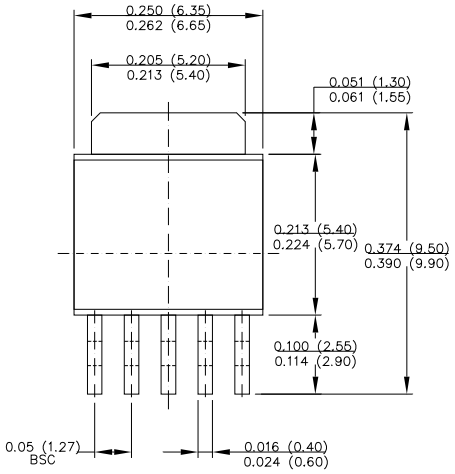


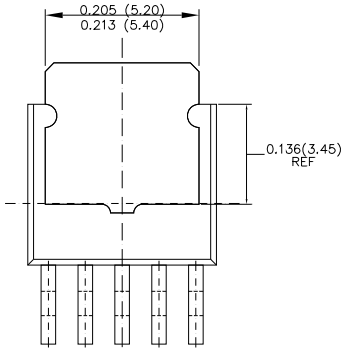
Figure 5: Typical Application Circuit

PACKAGE INFORMATION

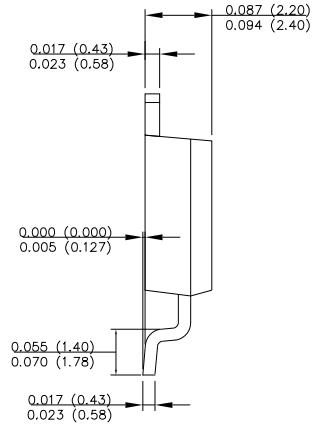
TO252-5



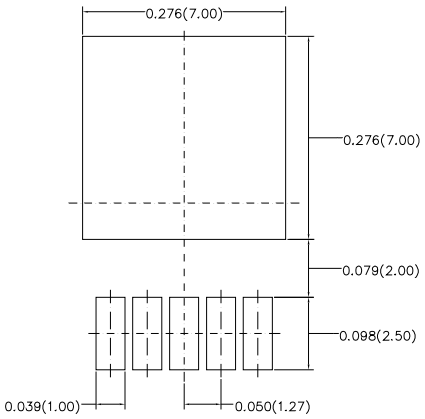
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) DRAWING CONFORMS TO JEDEC TO-252.
5) DRAWING IS NOT TO SCALE.