TVS Diode

Transient Voltage Suppressor Diodes

ESD3V3S1B Series

Ultra Low Clamping Bi-directional ESD / Transient Protection Diode

ESD3V3S1B-02LRH
ESD3V3S1B-02LS

Data Sheet

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Final

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Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Revision 1.1, 2011-11-28	
Revision 1.1; 2011-11-28	Features 1.1; Table 3-1; Table 3-3; Table 3-4

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1 Ultra Low Clamping Bi-directional ESD / Transient Protection Diode

1.1 Features

- ESD / transient protection of signal lines in low voltage applications according to:
  - IEC61000-4-2 (ESD): ±30 kV (contact)
  - IEC61000-4-4 (EFT): 40 A (5/50 ns)
  - IEC61000-4-5 (surge): 8 A (8/20 µs)
- Bi-directional, symmetrical working voltage up to V_{RWM} = ±3.3 V
- Ultra low clamping voltage V_{CL} = 7 V typ. @ I_{PP} = 16 A (TLP)
- Ultra low dynamic resistance R_{DYN} = 0.13 Ω typ.
- Smallest form factor: 0.62 x 0.32 x 0.31 mm^3
- Pb-free (RoHS compliant) and halogen free package

1.2 Application Examples

- Audio Line, Speaker, Headset, Microphone Protection
- Human Interface Devices (Keyboard, Touchpad, Buttons)

2 Product Description

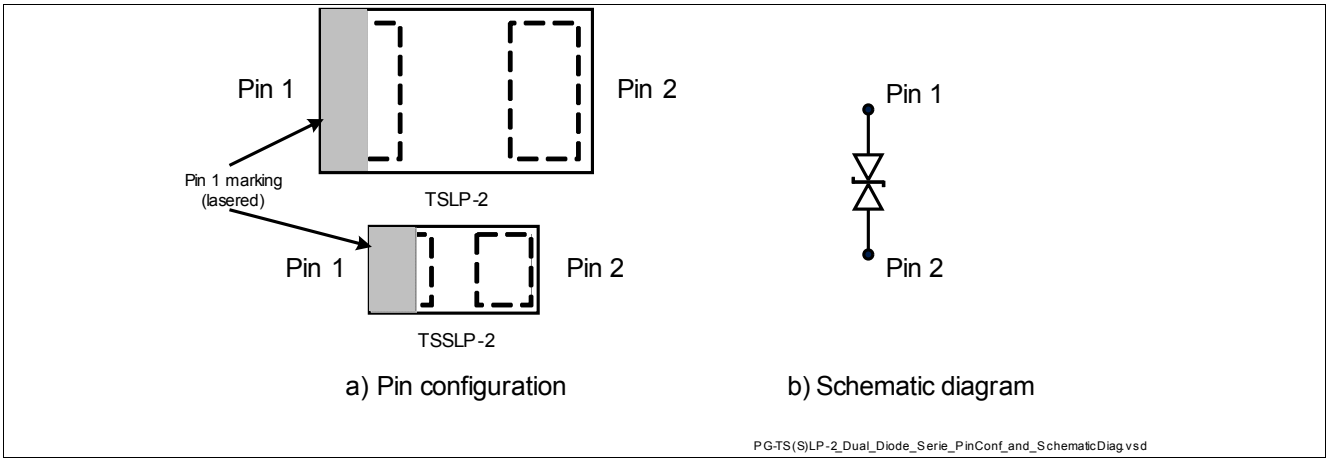


Figure 2-1 Pin Configuration and Schematic Diagram

Table 2-1 Ordering Information

Type	Package	Configuration	Marking code
ESD3V3S1B-02LRH	PG-TSLP-2-17	1 line, bi-directional	Y
ESD3V3S1B-02LS	PG-TSSLP-2-1	1 line, bi-directional	Y

3 Characteristics

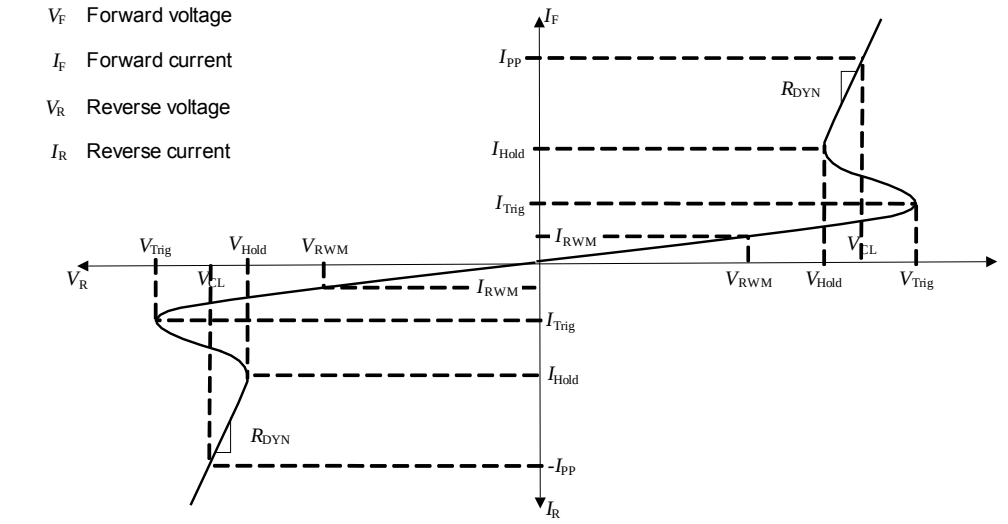
Table 3-1 Maximum Ratings at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
ESD contact discharge[1)]	V_{ESD}	–	–	30	kV
Peak pulse current (t_p = 8/20 µs)[2)]	I_{PP}	–	–	8	A
Operating temperature range	T_{OP}	-40	–	125	°C
Storage temperature	T_{stg}	-65	–	150	°C

1) V_{ESD} according to IEC61000-4-2

2) I_{PP} according to IEC61000-4-5

3.1 Electrical Characteristics at T_A = 25 °C, unless otherwise specified



R_{DYN}	Dynamic resistance	V_{FC}	Forward clamping voltage
V_{Trig}	Triggering reverse voltage	I_{Trig}	Triggering reverse current
V_{CL}	Clamping voltage	I_{Hold}	Holding reverse current
V_{Hold}	Holding reverse voltage	I_{PP}	Peak pulse current
V_{RWM}	Reverse working voltage maximum	I_{RWM}	Reverse working current maximum

Diode_Characteristic_Curve_with _snapback_Bi-directional.vsd

Figure 3-1 Definitions of electrical characteristics

Table 3-2 DC Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse working voltage	V_{RWM}	-3.3	–	3.3	V	
Reverse current	I_R	–	–	50	nA	V_R = 3.3 V

Table 3-3 RF Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance	C_L	–	14	20	pF	V_R = 0 V, f = 1 MHz

Table 3-4 ESD Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage[1)]	V_{CL}	–	7	–	V	I_{PP} = 16 A, t_p = 100 ns
		–	9	–	V	I_{PP} = 30 A, t_p = 100 ns
Clamping voltage[2)]	V_{CL}	–	4.5	–	V	I_{PP} = 1 A, t_p = 8/20 µs
		–	6.8	–	V	I_{PP} = 8 A, t_p = 8/20 µs
Dynamic resistance[1)]	R_{DYN}	–	0.13	–	Ω	

1) Please refer to Application Note AN210 [1]. TLP parameter: Z_0 = 50 Ω, t_p = 100ns, t_r = 300ps, averaging window: t_1 = 30 ns to t_2 = 60 ns, extraction of dynamic resistance using least squares fit of TLP charactertistics between I_{PP1} = 10 A and I_{PP2} = 40 A.

2) I_{PP} according to IEC61000-4-5

3.2 Typical Characteristics at T_A = 25 °C, unless otherwise specified

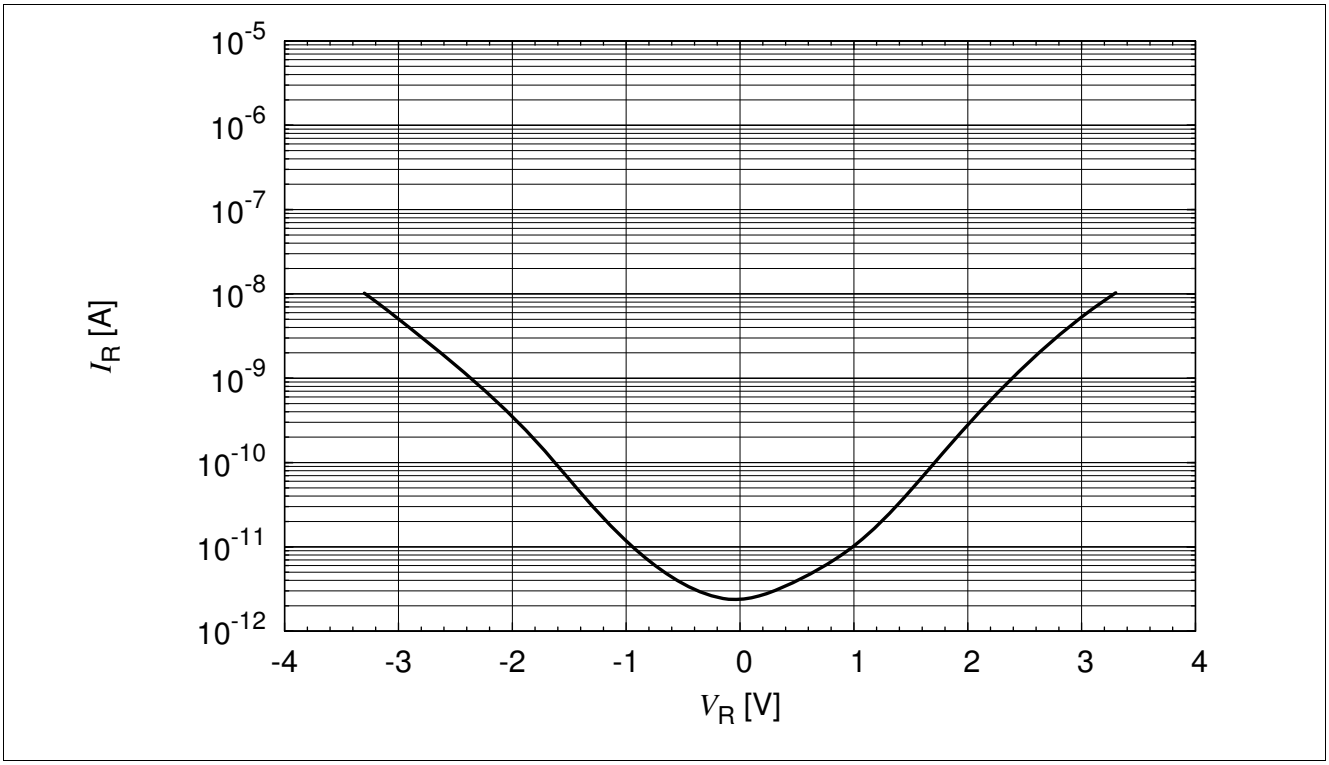


Figure 3-2 Reverse current: $I_R = f(V_R)$

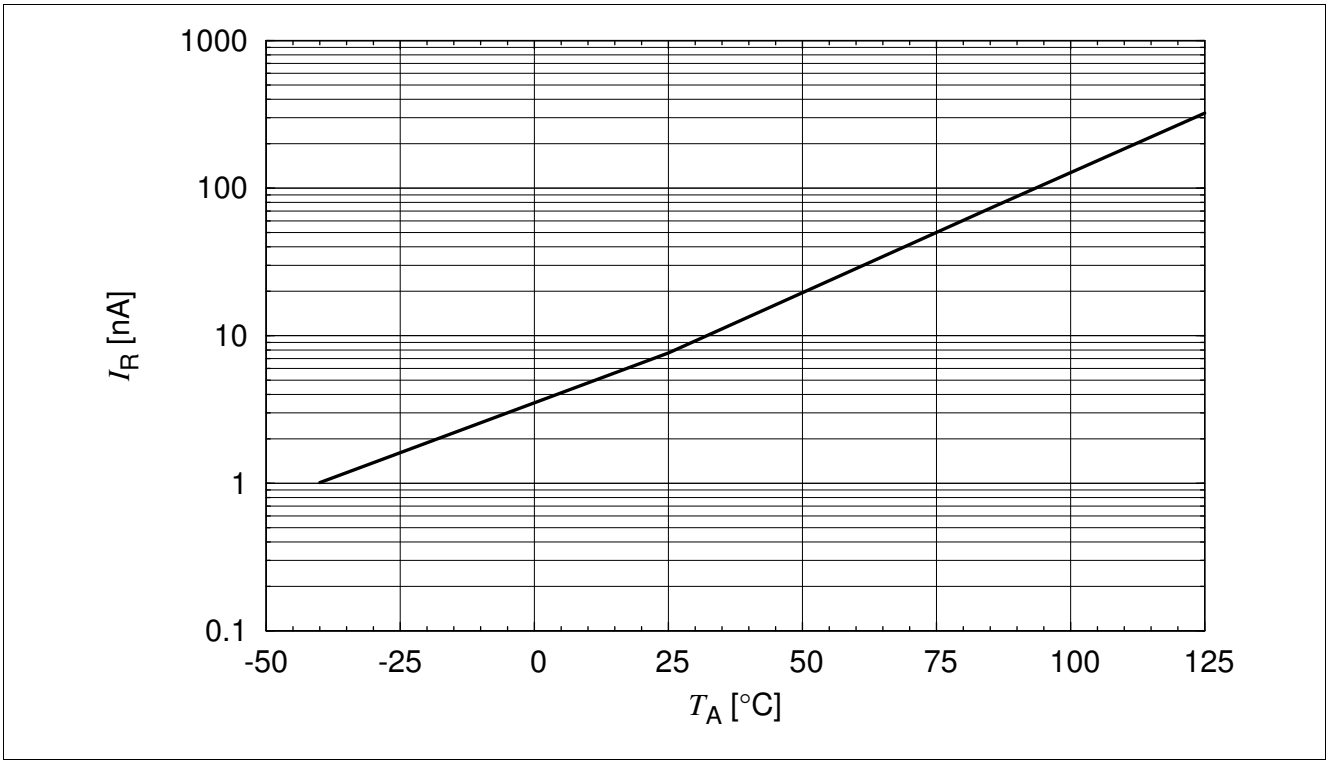


Figure 3-3 Reverse current: $I_R = f(T_A)$, $V_R = 3.3\ V$

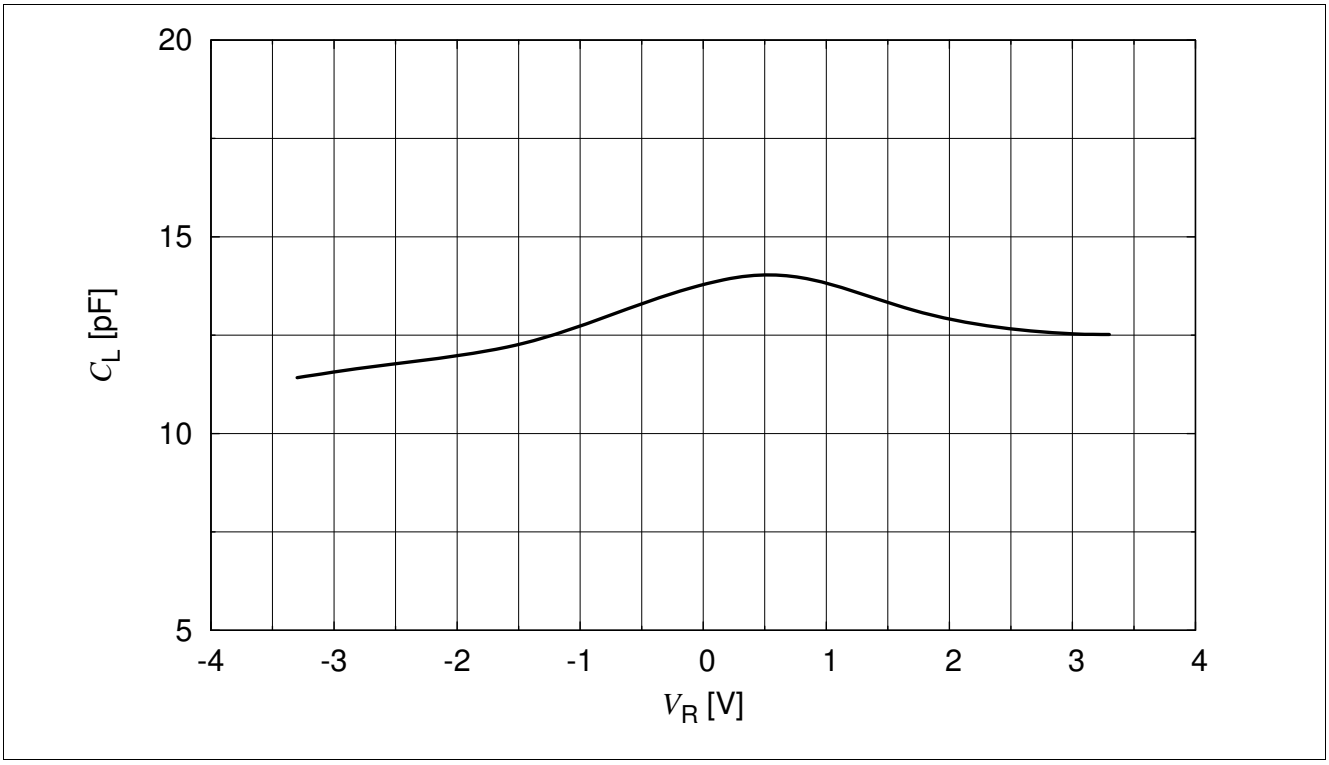


Figure 3-4 Line capacitance: $C_L = f(V_R)$, f = 1MHz

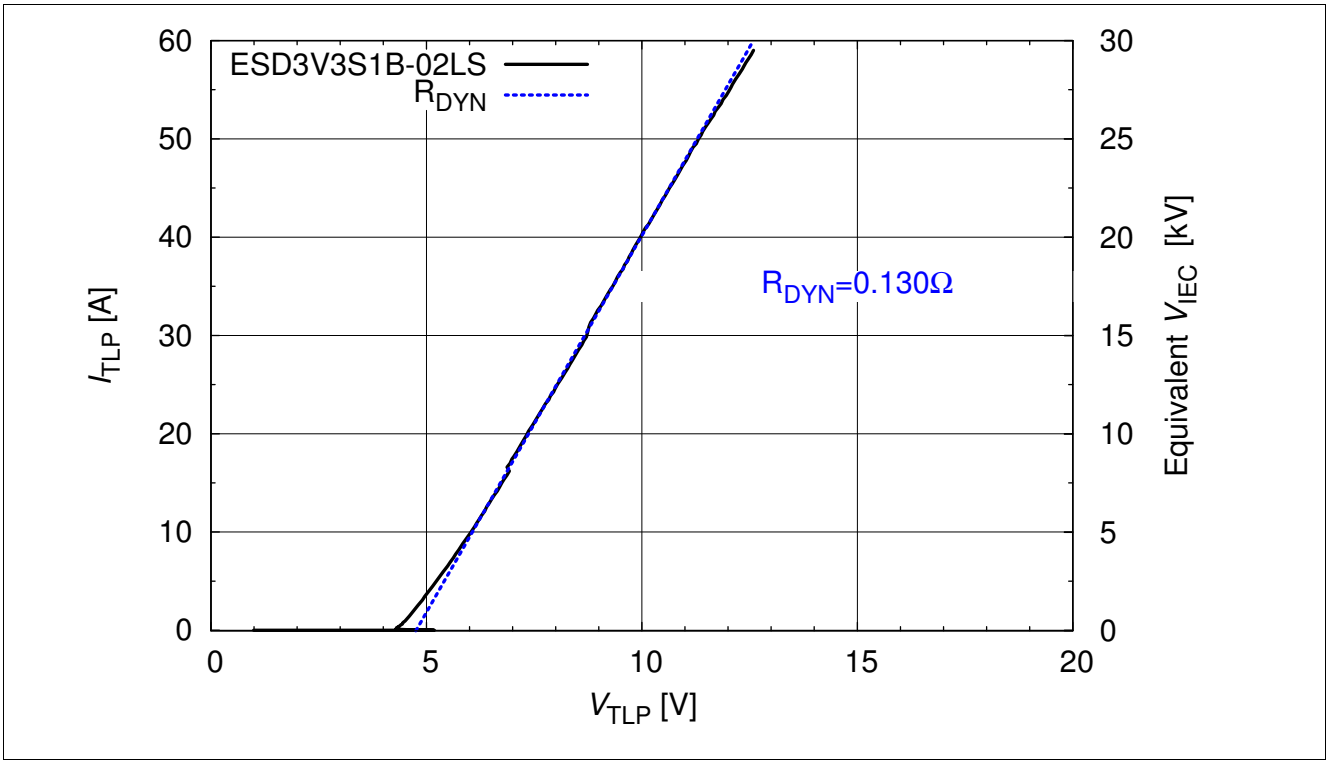


Figure 3-5 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$, from pin 1 to pin 2 [1]

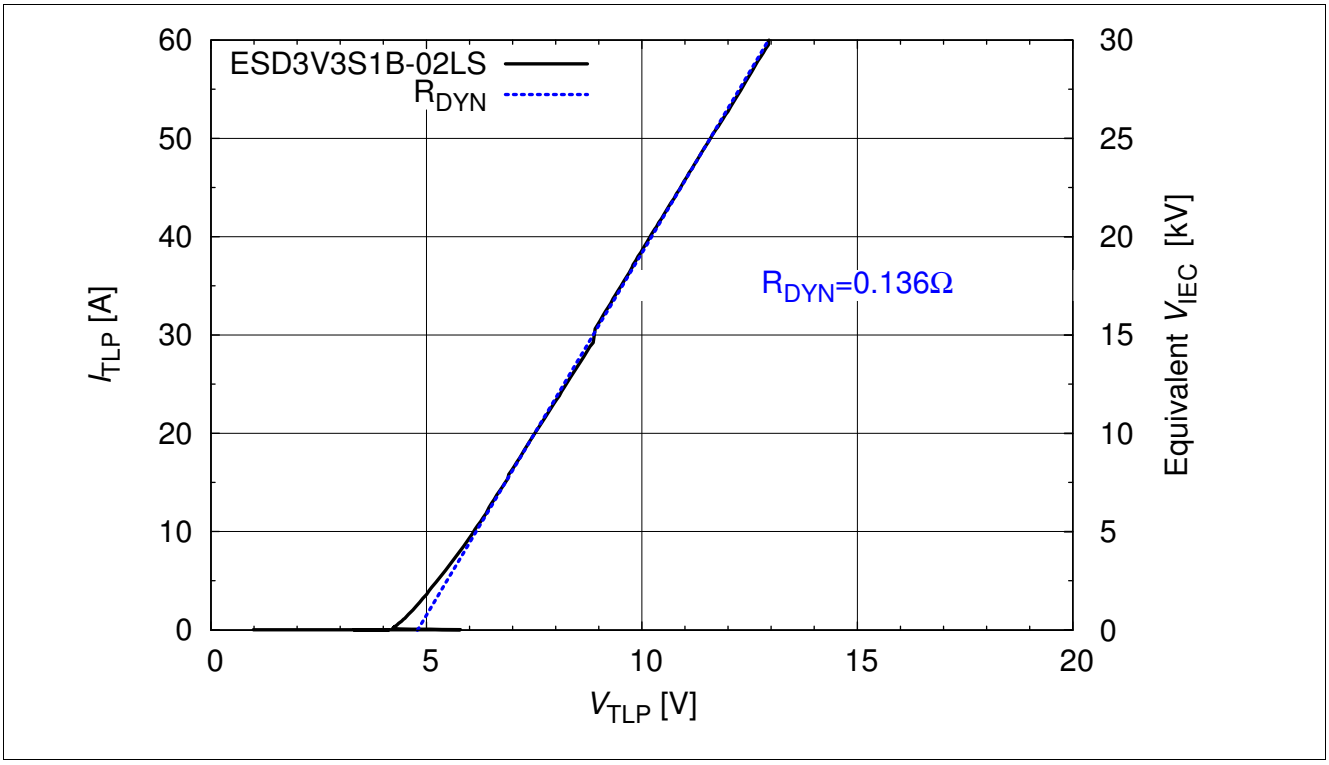


Figure 3-6 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$, from pin 2 to pin 1 [1]

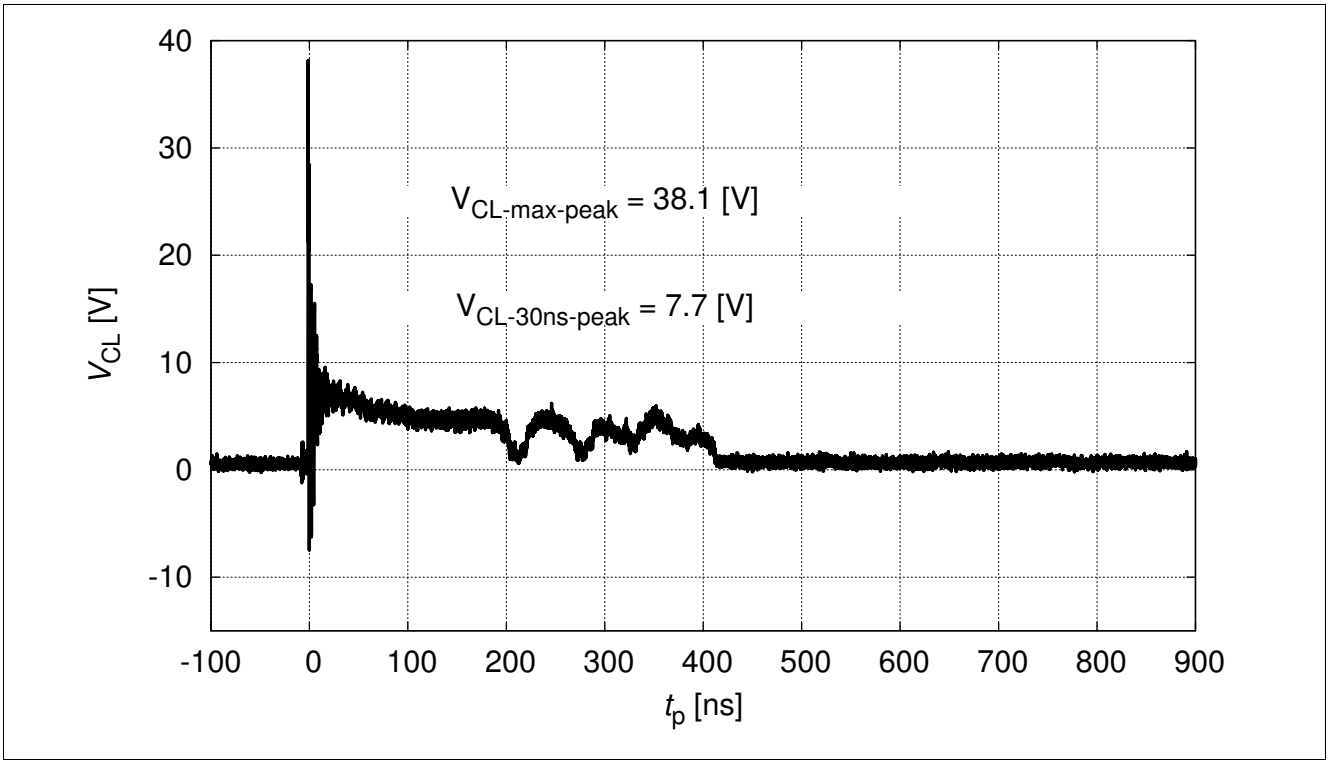


Figure 3-7 IEC61000-4-2 : V_{CL} = $f(t)$, 8 kV positive pulse from pin 1 to pin 2

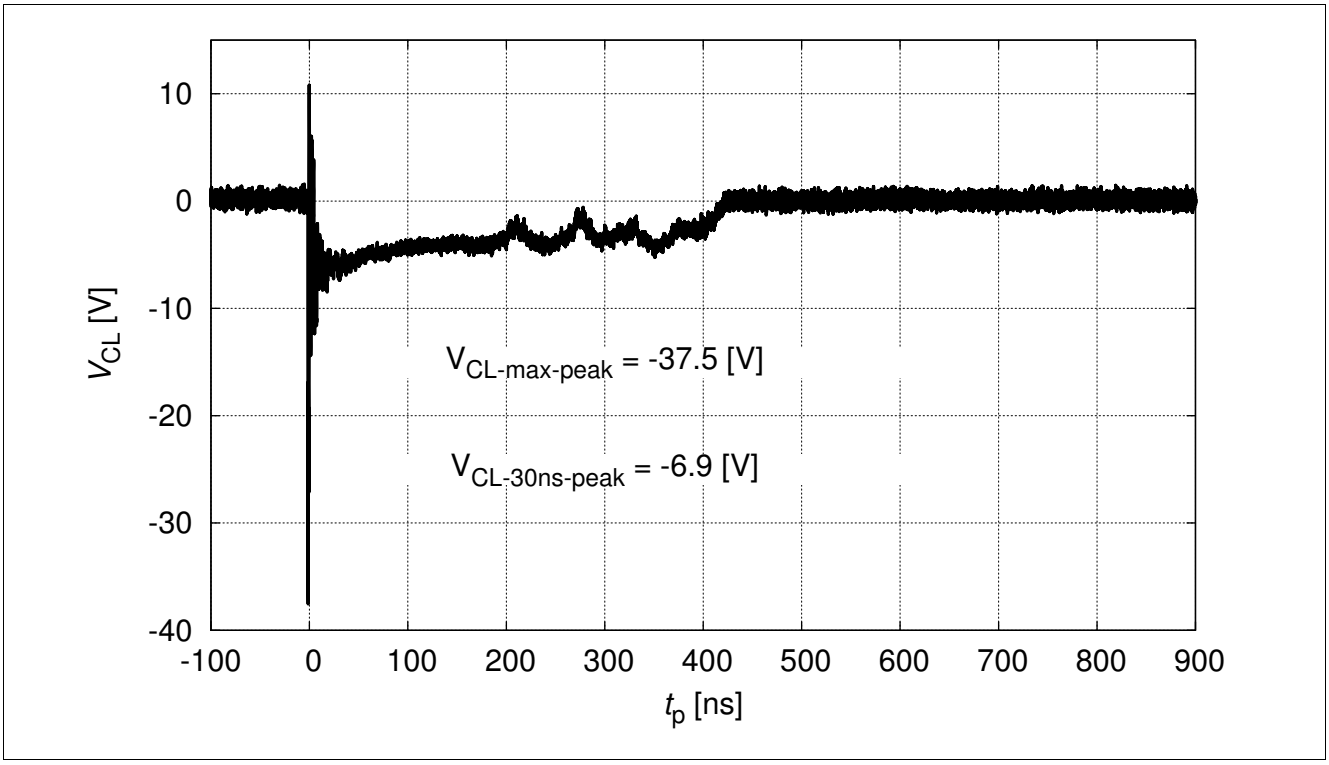


Figure 3-8 IEC61000-4-2 : V_{CL} = $f(t)$, 8 kV negative pulse from pin 1 to pin 2

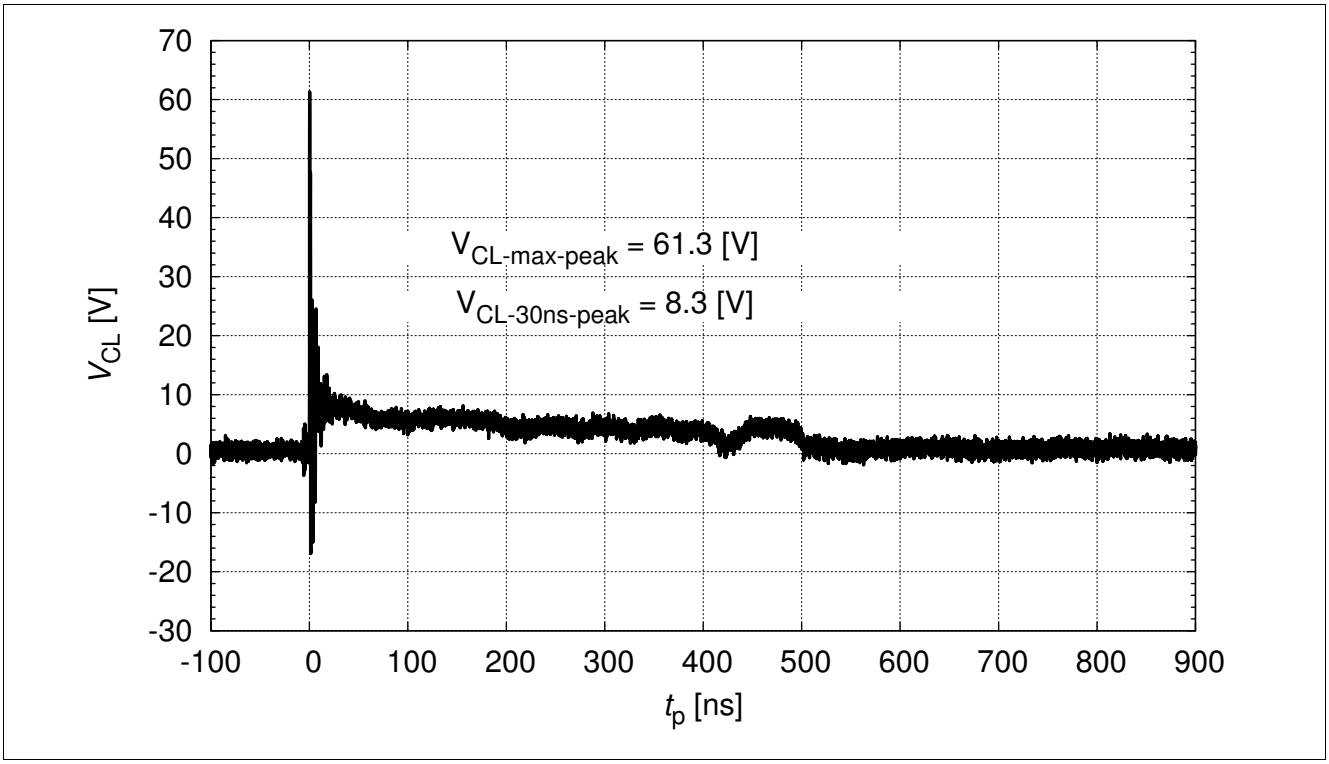


Figure 3-9 IEC61000-4-2 : V_{CL} = $f(t)$, 15 kV positive pulse from pin 1 to pin 2

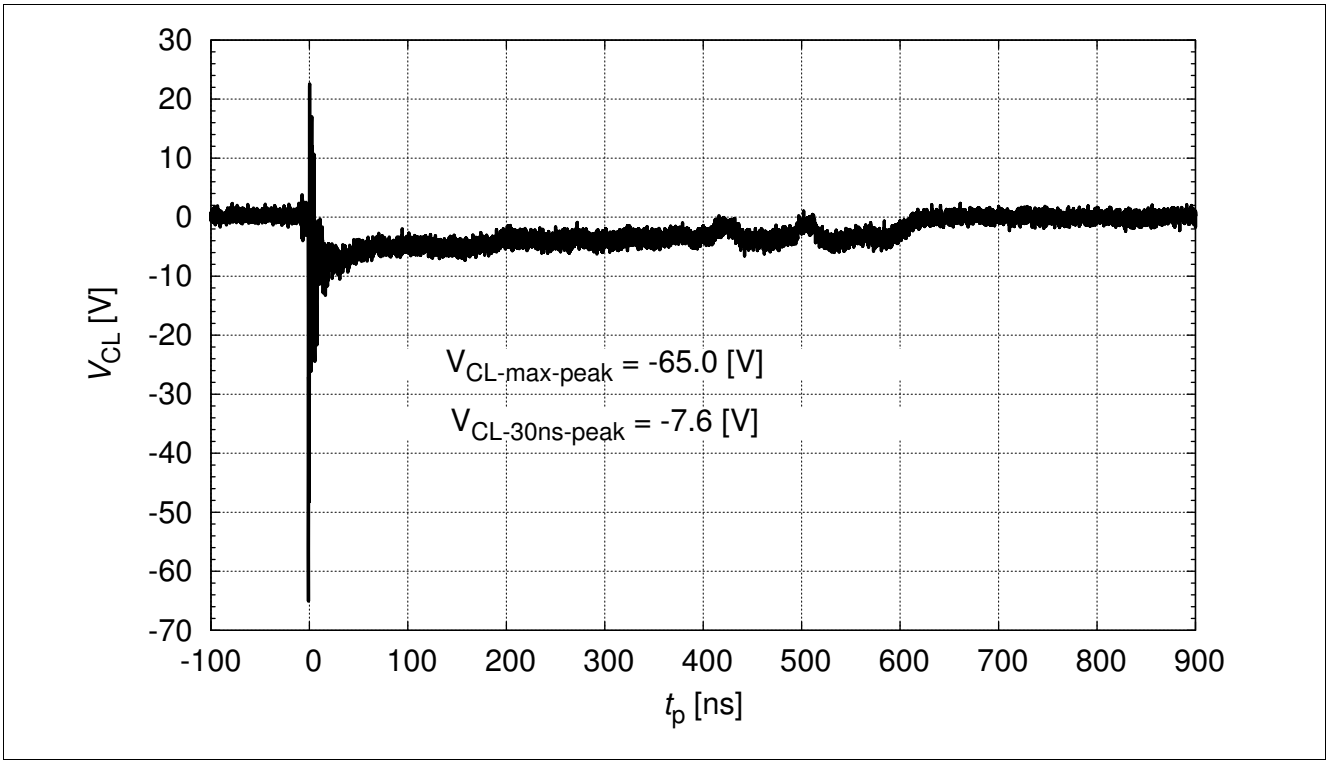


Figure 3-10 IEC61000-4-2 : V_{CL} = $f(t)$, 15 kV negative pulse from pin 1 to pin 2

4 Application Information

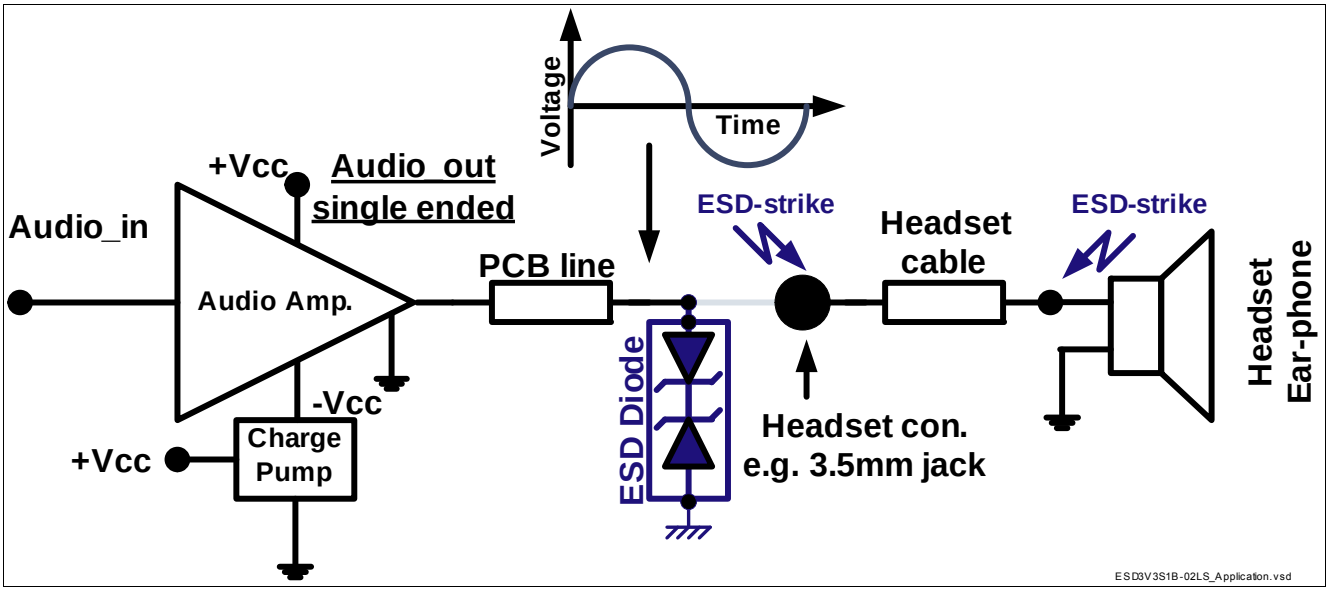


Figure 4-1 Single line, bi-directional ESD / Transient protection

5 Ordering Information Scheme (Examples)

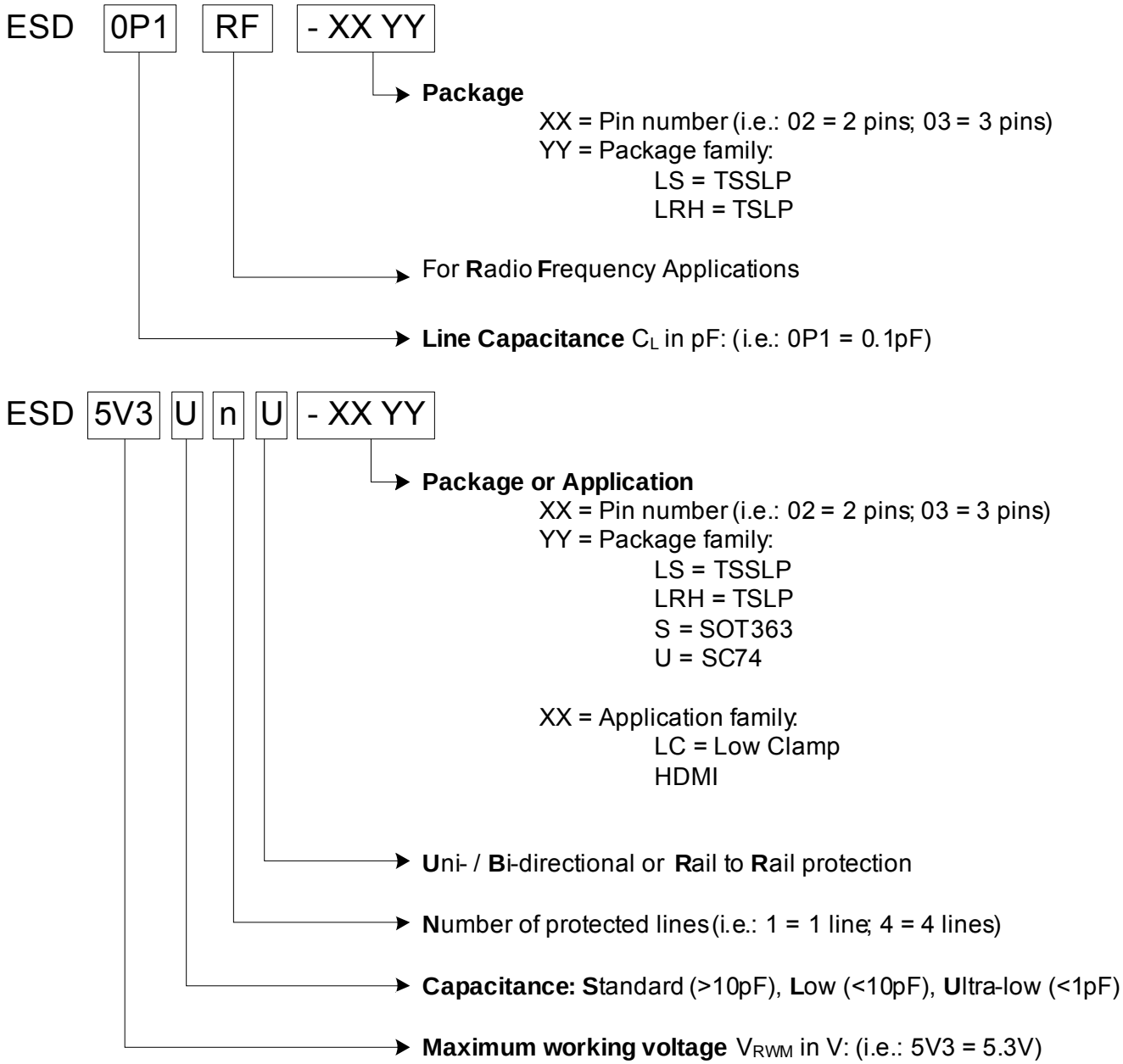


Figure 5-1 Ordering information scheme

6 Package Information

6.1 PG-TSLP-2-17 (mm) [2]

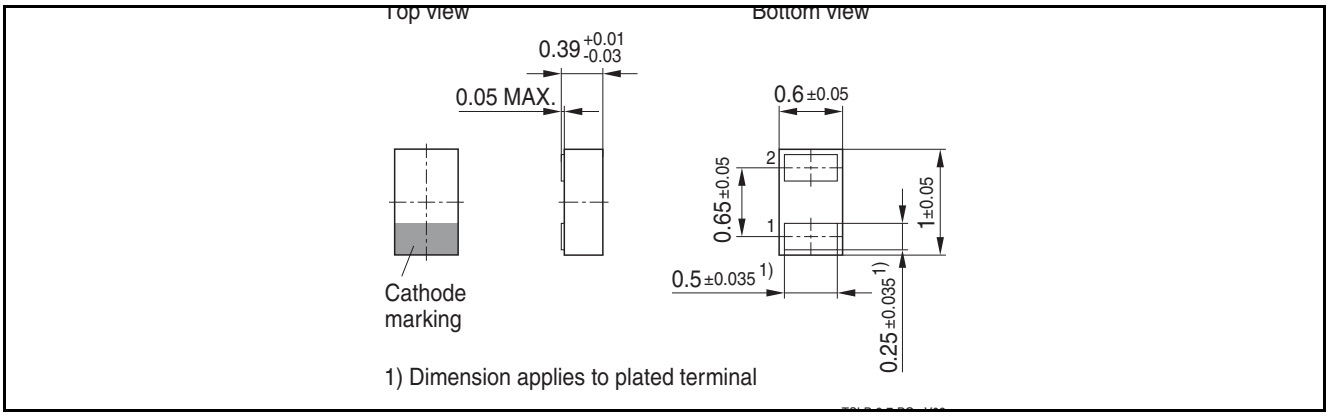


Figure 6-1 PG-TSLP-2-17: Package overview

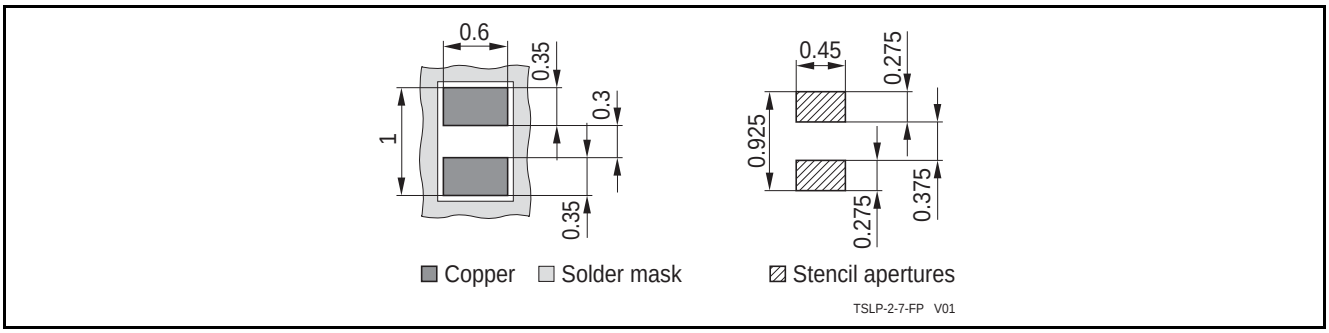


Figure 6-2 PG-TSLP-2-17: Footprint

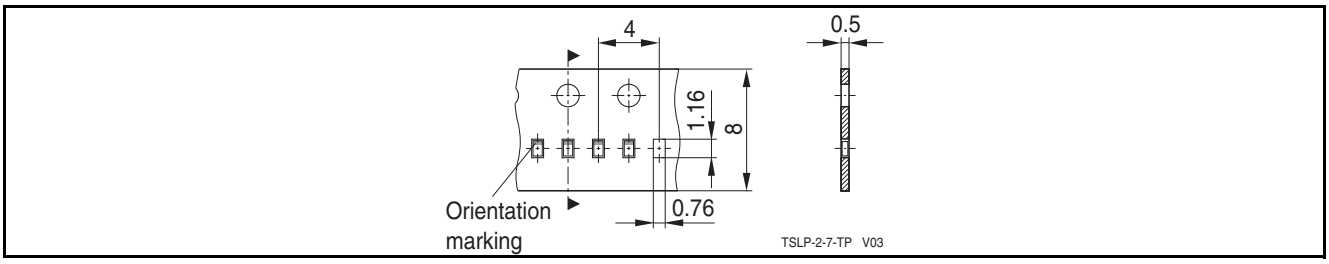


Figure 6-3 PG-TSLP-2-17: Packing

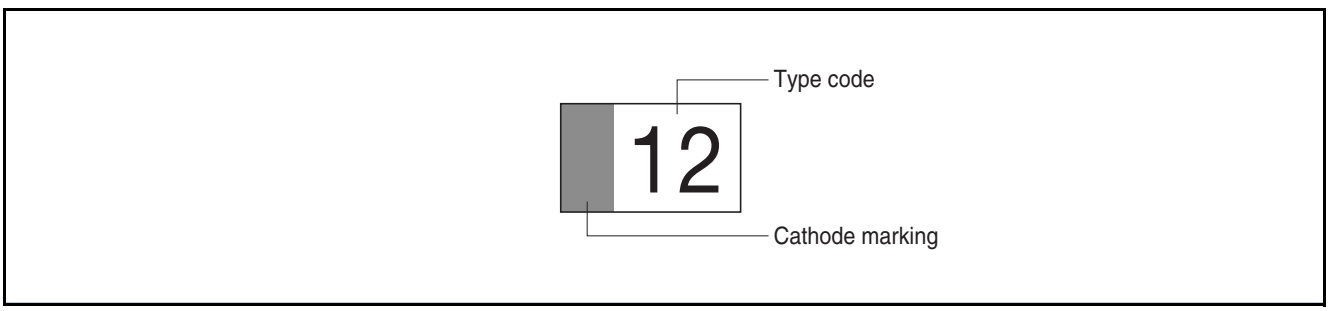


Figure 6-4 PG-TSLP-2-17: Marking (example)

6.2 PG-TSSLP-2-1 (mm) [2]

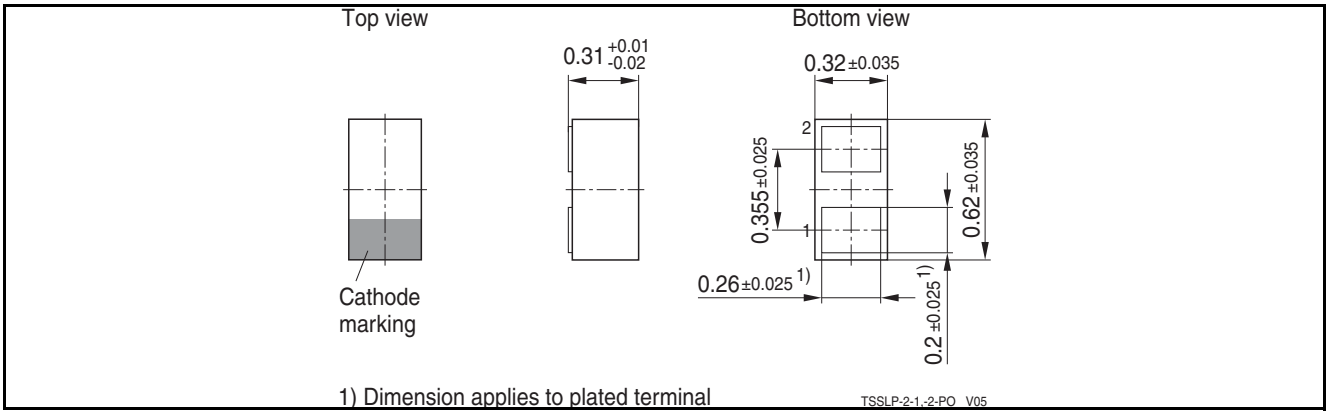


Figure 6-5 PG-TSSLP-2-1: Package overview

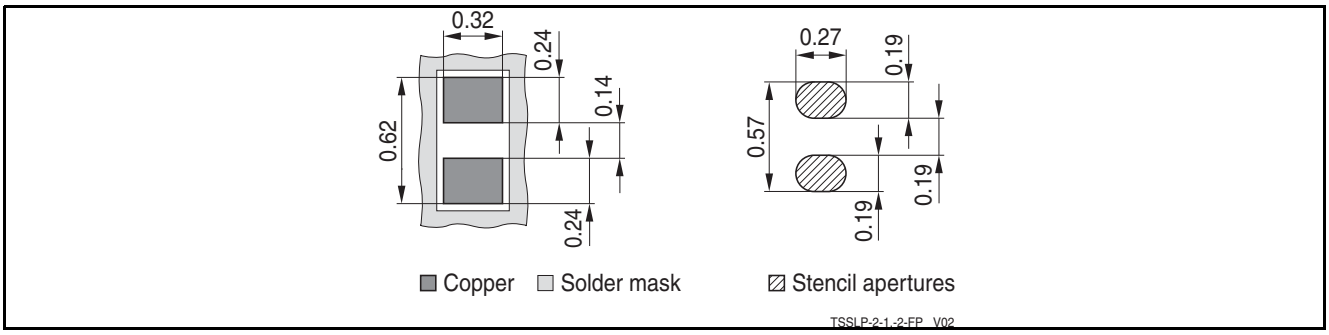


Figure 6-6 PG-TSSLP-2-1: Footprint

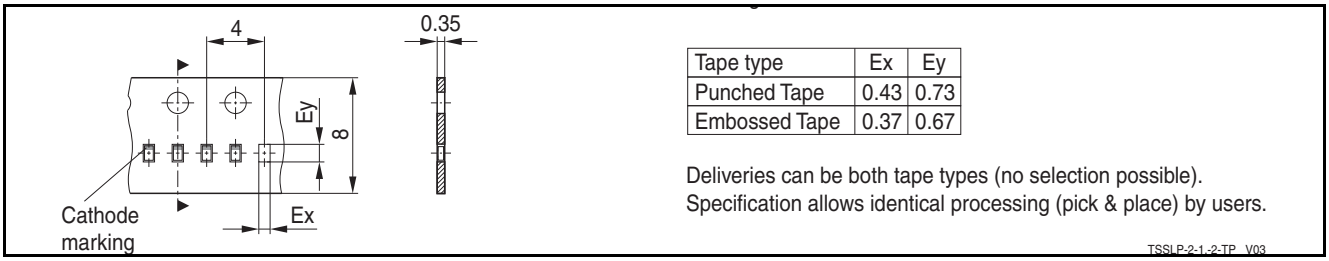


Figure 6-7 PG-TSSLP-2-1: Packing

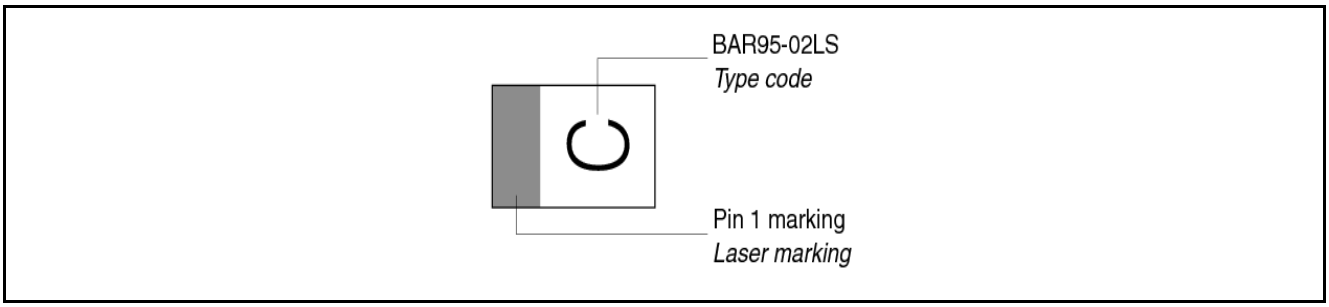


Figure 6-8 PG-TSSLP-2-1: Marking (example)

References

[1] Infineon AG - **Application Note AN210:** Effective ESD Protection design at System Level Using VF-TLP Characterization Methodology

[2] Infineon AG - Recommendations for PCB Assembly of Infineon TSLP and TSSLP Packages

Terminology

C_L	Line capacitance
EFT	Electrical Fast Transient
ESD	Electrostatic Discharge
I_{PP}	Peak pulse current
I_R	Reverse current
LCD	Liquid Crystal Display
$\boldsymbol{P_{PK}}$	Peak pulse power
R_{DYN}	Dynamic resistance
RoHs	Restriction of Hazardous Substance directive
T_A	Ambient temperature
T_{OP}	Operation temperature
t_p	Pulse duration
T_{stg}	Storage temperature
V_{BR}	Breakdown voltage
V_{CL}	Reverse clamping voltage
V_{ESD}	Electrostatic discharge voltage
V_R	Reverse voltage
V_{RWM}	Reverse working voltage maximum

Predefined Names

Name	Initial Cross-Reference
X-GOLD	**X-GOLD**
XMM	**XMM**

Definition of “Predefined Names”

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