FEATURES

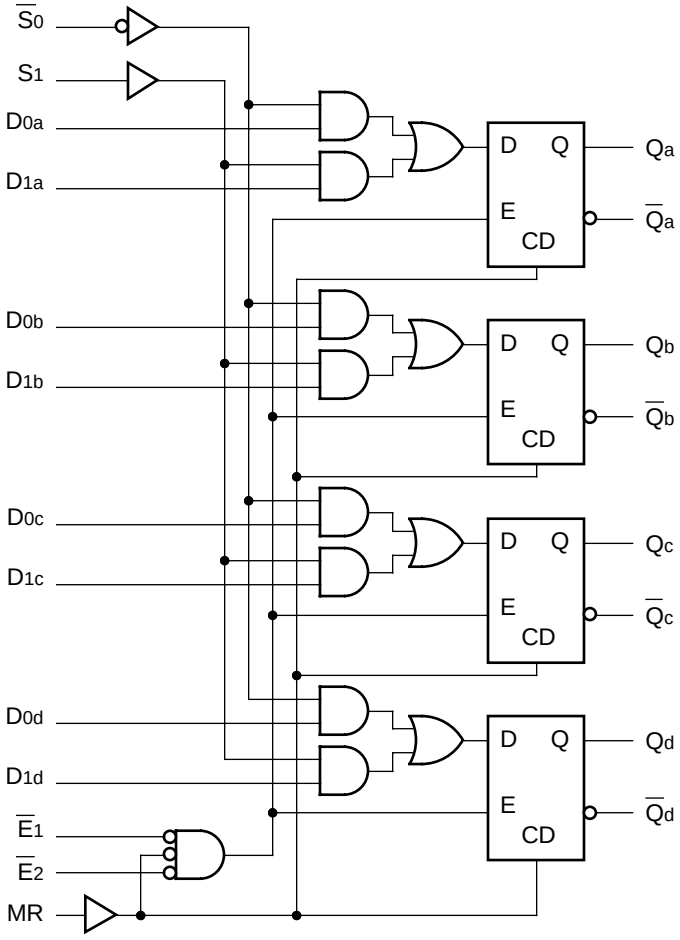
- **Max. propagation delay of 1100ps**
- **Max. enable to output delay of 1400ps**
- **I_{EE} min. of –80mA**
- **Industry standard 100K ECL levels**
- **Extended supply voltage option: V_{EE} = –4.2V to –5.5V**
- **Voltage and temperature compensation for improved noise immunity**
- **Internal 75kΩ input pull-down resistors**
- **50% faster than Fairchild**
- **Function and pinout compatible with Fairchild F100K**
- **Available in 28-pin PLCC package**

DESCRIPTION

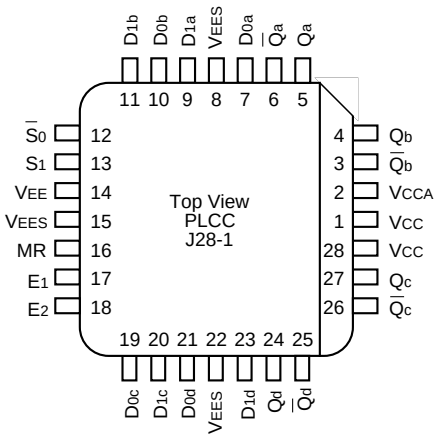
The SY100S355 offers four transparent latches with differential outputs and is designed for use in high-performance ECL systems. The Select inputs ($\overline{S}_0$, S_1) select one of the two sources of input data (D_0 or D_1) to the latch. The Select inputs can also force the outputs to a logic LOW when the latch is in the transparent mode. The latches are in the transparent mode when both Enables ($\overline{E}_1$, $\overline{E}_2$) are at a logic LOW state. In the transparent mode, the Select inputs can pass an input logic HIGH from D_0 or D_1 to the output.

If the Select inputs are tied together, then input data from either D_0 or D_1 is always passed through. A rising edge on either Enable input will latch the outputs with the most recent data at the latch inputs being stored. The Master Reset (MR) input overrides all other inputs and takes the Q outputs to a logic LOW. The inputs on this device have 75kΩ pull-down resistors.

BLOCK DIAGRAM



PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S355JC	J28-1	Commercial	SY100S355JC	Sn-Pb
SY100S355JCTR[1]	J28-1	Commercial	SY100S355JC	Sn-Pb
SY100S355JZ[2]	J28-1	Commercial	SY100S355JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S355JZTR[1, 2]	J28-1	Commercial	SY100S355JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Tape and Reel.
2. Pb-Free package is recommended for new designs.

PIN NAMES

Pin	Function
$\overline{E}_1 - \overline{E}_2$	Enable Inputs (Active LOW)
$\overline{S}_0$, S_1	Select Inputs
MR	Master Reset
$D_{na} - D_{nd}$	Data Inputs
$Q_a - Q_d$	Data Outputs
$\overline{Q}_a$ — $\overline{Q}_d$	Complementary Data Outputs
V_{EES}	V_{EE} Substrate
V_{CCA}	V_{CCO} for ECL Outputs

TRUTH TABLE[1]

Inputs							Outputs	
MR	$\overline{E}_1$	$\overline{E}_2$	S_1	$\overline{S}_0$	D_{1X}	D_{0X}	$\overline{Q}_X$	Q_X
H	X	X	X	X	X	X	H	L
L	L	L	H	H	H	X	L	H
L	L	L	H	H	L	X	H	L
L	L	L	L	L	X	H	L	H
L	L	L	L	L	X	L	H	L
L	L	L	L	H	X	X	H	L
L	L	L	H	L	H	X	L	H
L	L	L	H	L	X	H	L	H
L	L	L	H	L	L	L	H	L
L	H	X	X	X	X	X	Latched	
L	X	H	X	X	X	X	Latched	

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care

DC ELECTRICAL CHARACTERISTICS

V_{EE} = –4.2V to –5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND

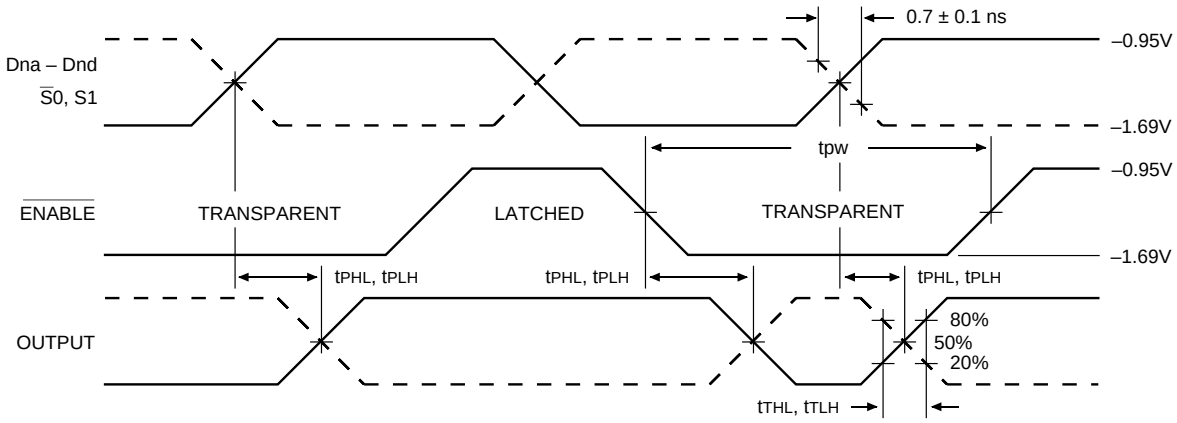
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current				µA	V_{IN} = V_{IH} (Max.)
	$\overline{S}_0$, S_1	—	—	220		
	$\overline{E}_1$, $\overline{E}_2$	—	—	350		
	D_{na}, D_{nd}	—	—	340		
	MR	—	—	430		
I_{EE}	Power Supply Current	–80	–57	–40	mA	Inputs Open

AC ELECTRICAL CHARACTERISTICS

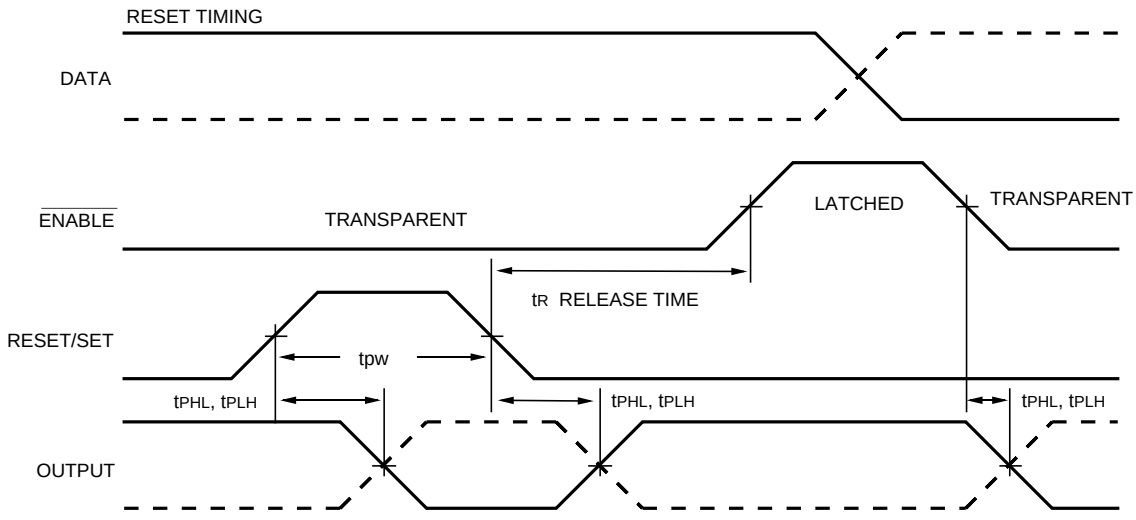
V_{EE} = –4.2V to –5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND

		T_A = 0°C		T_A = +25°C		T_A = +85°C			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay D_{na} – D_{nd} to Output (Transparent Mode)	300	1100	300	1100	300	1100	ps	
t_{PLH} t_{PHL}	Propagation Delay $\overline{S}_0$, S_1 to Output (Transparent Mode)	300	1400	300	1400	300	1400	ps	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$, $\overline{E}_2$ to Output	300	1400	300	1400	300	1400	ps	
t_{PLH} t_{PHL}	Propagation Delay MR to Output	300	1100	300	1100	300	1100	ps	
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
t_S	Set-up Time							ps	
	D_{na} – D_{nd}	700	—	700	—	700	—		
	$\overline{S}_0$, S_1	1200	—	1200	—	1200	—		
	MR (Release Time)	1000	—	1000	—	1000	—		
t_H	Hold Time							ps	
	D_{na} – D_{nd}	300	—	300	—	300	—		
	$\overline{S}_0$, S_1	300	—	300	—	300	—		
t_{PW} (L)	Pulse Width LOW, $\overline{E}_1$, $\overline{E}_2$	1000	—	1000	—	1000	—	ps	
t_{PW} (H)	Pulse Width HIGH, MR	1000	—	1000	—	1000	—	ps	

TIMING DIAGRAMS

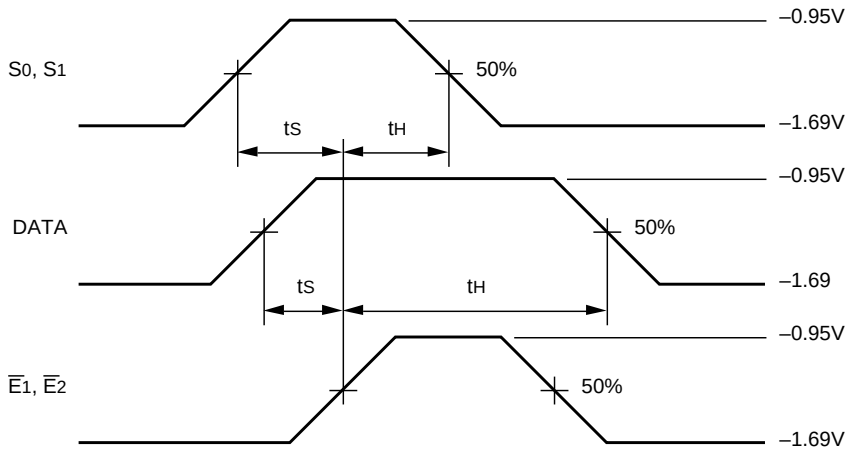


Enable Timing



Reset Timing

TIMING DIAGRAMS

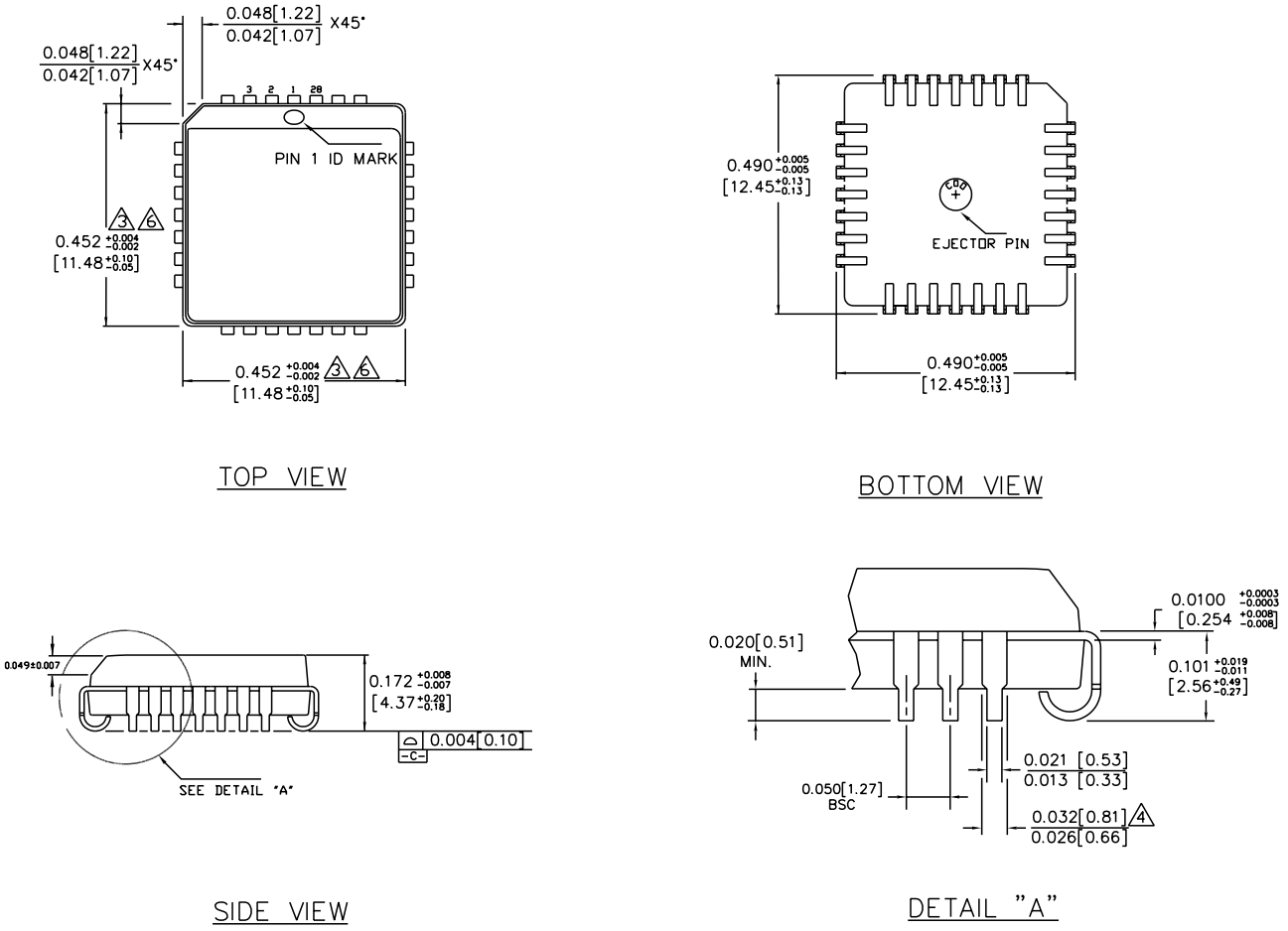


Data Set-up and Hold Times

Notes:

1. V_{EE} = –4.2V to –5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND
2. ts is the minimum time before the transition of the clock that information must be present at the data input.
3. t_H is the minimum time after the transition of the clock that information must remain unchanged at the data input.

28-PIN PLCC (J28-1)



Rev. A

NOTES:
1. DIMENSIONS ARE IN INCHES [MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

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