

FEATURES

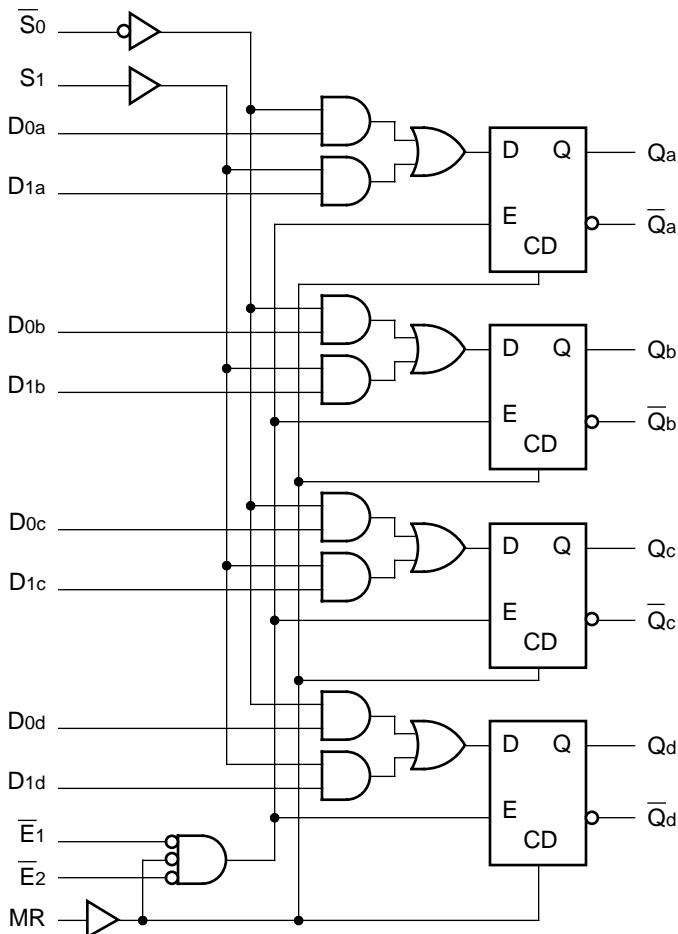
- Max. propagation delay of 1100ps
- Max. enable to output delay of 1400ps
- IEE min. of -80mA
- Industry standard 100K ECL levels
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75kΩ input pull-down resistors
- 50% faster than Fairchild
- Function and pinout compatible with Fairchild F100K
- Available in 28-pin PLCC package

DESCRIPTION

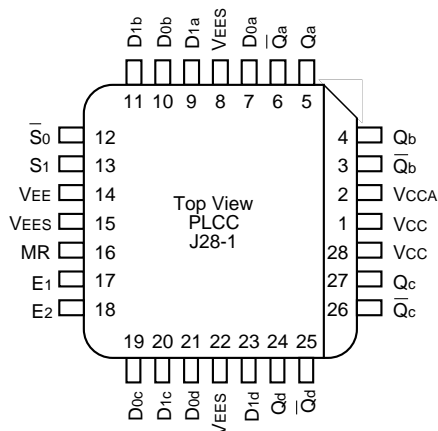
The SY100S355 offers four transparent latches with differential outputs and is designed for use in high-performance ECL systems. The Select inputs (\bar{S}_0 , S_1) select one of the two sources of input data (D_0 or D_1) to the latch. The Select inputs can also force the outputs to a logic LOW when the latch is in the transparent mode. The latches are in the transparent mode when both Enables (\bar{E}_1 , \bar{E}_2) are at a logic LOW state. In the transparent mode, the Select inputs can pass an input logic HIGH from D_0 or D_1 to the output.

If the Select inputs are tied together, then input data from either D_0 or D_1 is always passed through. A rising edge on either Enable input will latch the outputs with the most recent data at the latch inputs being stored. The Master Reset (MR) input overrides all other inputs and takes the Q outputs to a logic LOW. The inputs on this device have 75kΩ pull-down resistors.

BLOCK DIAGRAM



PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S355JC	J28-1	Commercial	SY100S355JC	Sn-Pb
SY100S355JCTR ⁽¹⁾	J28-1	Commercial	SY100S355JC	Sn-Pb
SY100S355JZ ⁽²⁾	J28-1	Commercial	SY100S355JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S355JZTR ^(1, 2)	J28-1	Commercial	SY100S355JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Tape and Reel.
2. Pb-Free package is recommended for new designs.

PIN NAMES

Pin	Function
$\bar{E}_1 - \bar{E}_2$	Enable Inputs (Active LOW)
\bar{S}_0, S_1	Select Inputs
MR	Master Reset
$D_{na} - D_{nd}$	Data Inputs
$Q_a - Q_d$	Data Outputs
$\bar{Q}_a - \bar{Q}_d$	Complementary Data Outputs
VEES	VEE Substrate
VCCA	VCCO for ECL Outputs

TRUTH TABLE⁽¹⁾

Inputs							Outputs	
MR	\bar{E}_1	\bar{E}_2	S_1	S_0	D_{1x}	D_{0x}	\bar{Q}_x	Q_x
H	X	X	X	X	X	X	H	L
L	L	L	H	H	H	X	L	H
L	L	L	H	H	L	X	H	L
L	L	L	L	L	X	H	L	H
L	L	L	L	L	X	L	H	L
L	L	L	H	L	H	X	L	H
L	L	L	H	L	X	H	L	H
L	H	X	X	X	X	X	Latched	Latched
L	X	H	X	X	X	X	Latched	Latched

NOTE:

1. H = High Voltage Level
L = Low Voltage Level
X = Don't Care

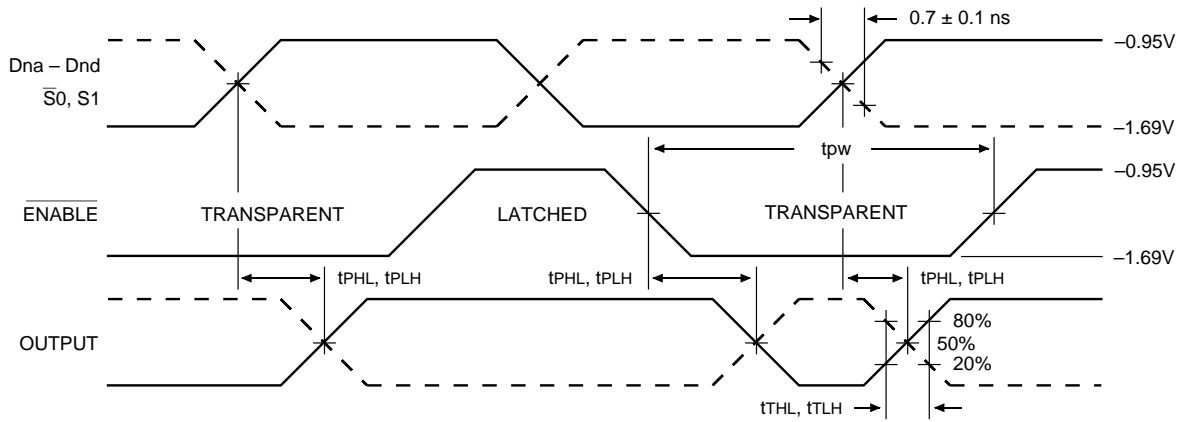
DC ELECTRICAL CHARACTERISTICSV_{EE} = -4.2V to -5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I _{IH}	Input HIGH Current S ₀ , S ₁ E ₁ , E ₂ D _{na} , D _{nd} MR	—	—	220 350 340 430	μA	V _{IN} = V _{IH} (Max.)
I _{EE}	Power Supply Current	-80	-57	-40	mA	Inputs Open

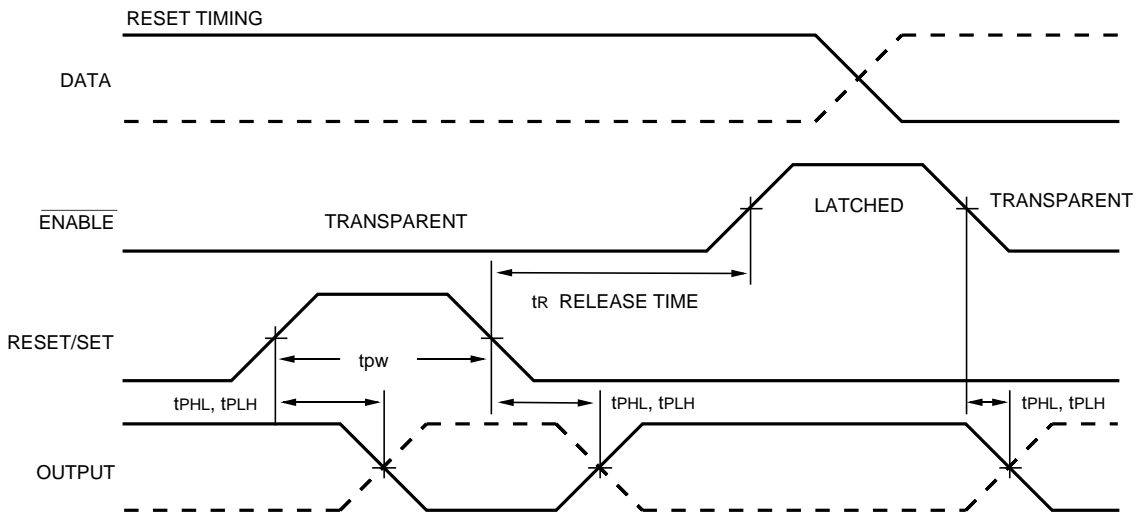
AC ELECTRICAL CHARACTERISTICSV_{EE} = -4.2V to -5.5V unless otherwise specified; V_{CC} = V_{CCA} = GND

Symbol	Parameter	T _A = 0°C		T _A = +25°C		T _A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay D _{na} – D _{nd} to Output (Transparent Mode)	300	1100	300	1100	300	1100	ps	
t _{PLH} t _{PHL}	Propagation Delay S ₀ , S ₁ to Output (Transparent Mode)	300	1400	300	1400	300	1400	ps	
t _{PLH} t _{PHL}	Propagation Delay E ₁ , E ₂ to Output	300	1400	300	1400	300	1400	ps	
t _{PLH} t _{PHL}	Propagation Delay MR to Output	300	1100	300	1100	300	1100	ps	
t _{TLH} t _{THL}	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
t _S	Set-up Time D _{na} – D _{nd} S ₀ , S ₁ MR (Release Time)	700 1200 1000	— — —	700 1200 1000	— — —	700 1200 1000	— — —	ps	
t _H	Hold Time D _{na} – D _{nd} S ₀ , S ₁	300 300	— —	300 300	— —	300 300	— —	ps	
t _{PW} (L)	Pulse Width LOW, E ₁ , E ₂	1000	—	1000	—	1000	—	ps	
t _{PW} (H)	Pulse Width HIGH, MR	1000	—	1000	—	1000	—	ps	

TIMING DIAGRAMS

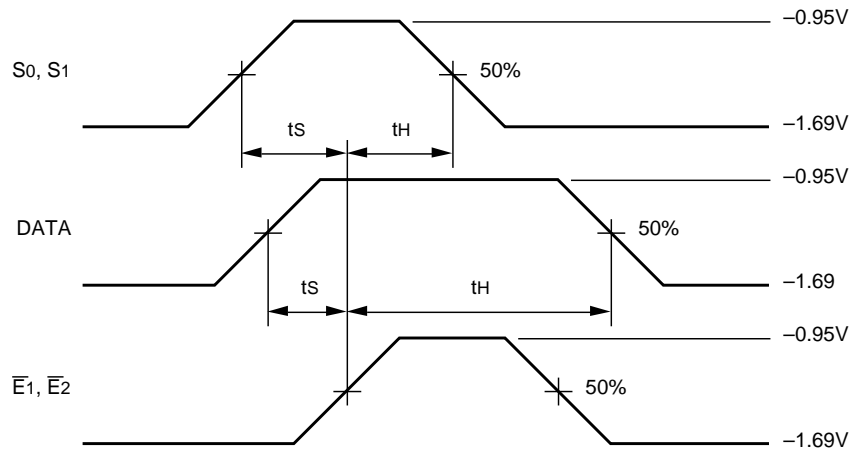


Enable Timing



Reset Timing

TIMING DIAGRAMS

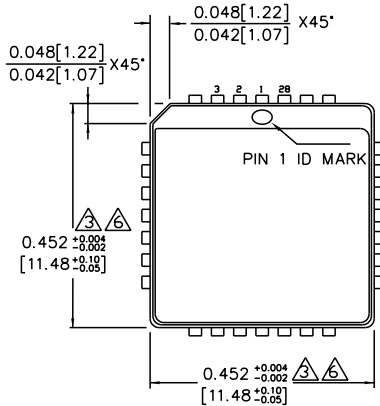


Data Set-up and Hold Times

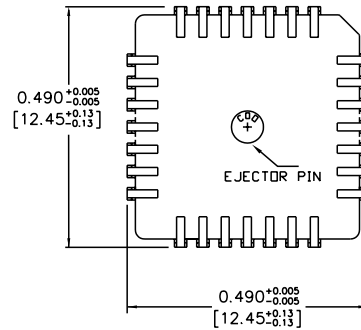
Notes:

1. $V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified; $V_{CC} = V_{CCA} = GND$
2. t_s is the minimum time before the transition of the clock that information must be present at the data input.
3. t_H is the minimum time after the transition of the clock that information must remain unchanged at the data input.

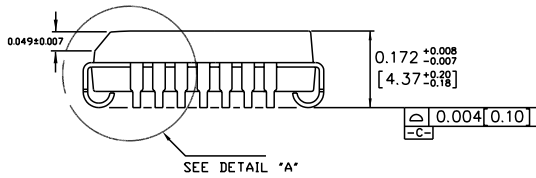
28-PIN PLCC (J28-1)



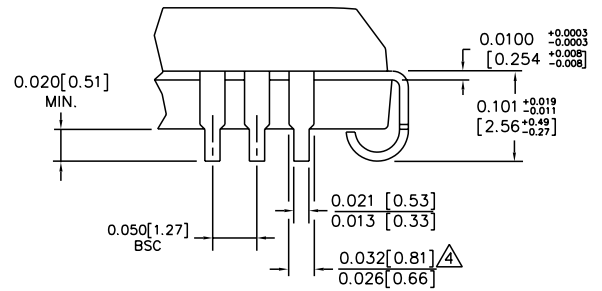
TOP VIEW



BOTTOM VIEW



SIDE VIEW



DETAIL "A"

NOTES:

1. DIMENSIONS ARE IN INCHES [MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. A

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL + 1 (408) 944-0800 FAX + 1 (408) 474-1000 WEB <http://www.micrel.com>

The information furnished by Micrel in this datasheet is believed to be accurate and reliable. However, no responsibility is assumed by Micrel for its use. Micrel reserves the right to change circuitry and specifications at any time without notification to the customer.

Micrel Products are not designed or authorized for use as components in life support appliances, devices or systems where malfunction of a product can reasonably be expected to result in personal injury. Life support devices or systems are devices or systems that (a) are intended for surgical implant into the body or (b) support or sustain life, and whose failure to perform can be reasonably expected to result in a significant injury to the user. A Purchaser's use or sale of Micrel Products for use in life support appliances, devices or systems is at Purchaser's own risk and Purchaser agrees to fully indemnify Micrel for any damages resulting from such use or sale.

© 2006 Micrel, Incorporated.