



TDA19978A

Quad HDMI 1.4a receiver interface with equalizer (HDTV up to 1080p, up to UXGA for PC's format)

Rev. 4 — 6 December 2010

Product data sheet

HDMI

1. General description

The TDA19978A is a four input HDMI 1.4a compliant receiver with embedded EDID memory. The built in auto-adaptive equalizer improves signal quality and allows the use of cable lengths up to 25 m (laboratory tested with a 0.5 mm (24 AWG) cable at 2.05 gigasamples per second). The HDCP key set is stored in non-volatile One Time Programmable (OTP) memory for maximum security. In addition, the TDA19978A is delivered with software drivers to ease configuration and use.

The TDA19978A supports:

- TV resolutions:
 - 480i (1440 × 480i at 60 Hz), 576i (1440 × 576i at 50 Hz) to HDTV (up to 1920 × 1080p at 50/60 Hz)
 - WUXGA (1920 × 1200p at 60 Hz) reduced blanking format
- PC resolutions:
 - VGA (640 × 480p at 60 Hz) to UXGA (1600 × 1200p at 60 Hz)
- Deep Color mode in 10-bit and 12-bit (up to 205 MHz TMDS clock)
- Gamut boundary description
- IEC 60958/IEC 61937, One Bit Audio (in SACD), DST (in compressed DSD) and HBR stream

The TDA19978A includes:

- An enhanced PC and TV format recognition system
- Generation of a $128/256/512 \times f_s$ system clock allowing the use of simple audio DACs without an integrated PLL (such as the UDA1334BTS)
- An embedded oscillator (an external crystal can also be used)
- Improved audio clock generation using an external reference clock
- One Bit Audio (in SACD), DST (in compressed DSD) and HBR stream support

The TDA19978A converts HDMI streams with or without HDCP into RGB or YCbCr digital signals. The YCbCr digital output signal can be 4:4:4 or 4:2:2 semi-planar format based on the ITU-R BT.601 standard or 4:2:2 based on the ITU-R BT.656 format. The device can adjust the output timing of the video port by altering the values for $t_{su(Q)}$ and $t_{h(Q)}$. In addition, all settings are controllable using the I²C-bus.



2. Features and benefits

- Complies with the HDMI 1.4a, DVI 1.0, CEA-861-D and HDCP 1.4 standards
- Four (quad) independent HDMI inputs, up to the HDMI frequency of 205 MHz
- Embedded auto-adaptive equalizer on all HDMI links
- EDID memory: 253 shared bytes and three bytes dedicated to each HDMI input
- Supports color depth processing (8-bit, 10-bit or 12-bit per color)
- Color gamut metadata packet with interrupt on each update, readable via the I²C-bus
- Up to four S/PDIF or I²S-bus outputs (eight channels) at a sampling rate up to 192 kHz with IEC 60958/IEC 61937 stream
- HBR audio stream up to 768 kHz with four demultiplexed S/PDIF or I²S-bus outputs
- HBR streams (compatible with DTS-HD master audio and Dolby TrueHD up to eight channels due to HBR packet for stream with a frame rate up to 768 kHz) support
- DSD and DST audio stream up to six DSD channels output for SACD with DST Audio Packet support
- Channel status decoder supports multi-channel reception
- Improved audio clock generation using an external reference clock
- System/master clock output ($128/256/512 \times f_s$) enables the use of the UDA1334BTS
- The HDMI interface supports:
 - ◆ All HDTV formats up to $1920 \times 1080p$ at 50/60 Hz and WUXGA ($1920 \times 1200p$ at 60 Hz) with support for reduced blanking
 - ◆ 3D formats including all primary formats up to $1920 \times 1080p$ at 30 Hz Frame Packing and $1920 \times 1080p$ at 60 Hz Top-and-Bottom
 - ◆ PC formats up to UXGA ($1600 \times 1200p$ at 60 Hz)
- Embedded oscillator (an external crystal can be used)
- Frame and field detection for interlaced video signal
- Sync timing measurements for format recognition
- Improved system for measurements of blanking and video active area allowing an accurate recognition of PC and TV formats
- HDCP with repeater capability
- Embedded non-volatile memory storage of HDCP keys
- Programmable color space input signal conversion from RGB-to-YCbCr or YCbCr-to-RGB
- Output formats: RGB 4:4:4, YCbCr 4:4:4, YCbCr 4:2:2 semi-planar based on the ITU-R BT.601 standard and YCbCr 4:2:2 ITU-R BT.656
- 8-bit, 10-bit or 12-bit output formats selectable using the I²C-bus (8-bit and 10-bit only in 4:4:4 format)
- I²C-bus adjustable timing of video port ($t_{su(Q)}$ and $t_{h(Q)}$)
- Downsampling-by-two with selectable filters on Cb and Cr channels in 4:2:2 mode
- Internal video and audio pattern generator
- Controllable using the I²C-bus; 5 V tolerant and bit rate up to 400 kbit/s
- DDC-bus inputs 5 V tolerant and bit rate up to 400 kbit/s
- LV-TTL outputs
- Power-down mode
- CMOS process
- 1.8 V and 3.3 V power supplies

- Lead-free (Pb) HLQFP144 package

3. Applications

- HDTV
- YCbCr or RGB HI-Speed video digitizer
- Projector, plasma and LCD TV
- Rear projection TV
- High-End TV
- Home theater amplifier
- DVD recorder
- AVR and HDMI splitter

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Digital inputs: pins RXxC+, RXxC- [1]						
$f_{clk(max)}$	maximum clock frequency		205	-	-	MHz
Clock timing output: pins VCLK, ACLK and SYSCLK						
$f_{clk(max)}$	maximum clock frequency	pin VCLK	165	-	-	MHz
		pin ACLK	25	-	-	MHz
		pin SYSCLK	50	-	-	MHz
Supplies						
$V_{DDH(3V3)}$	HDMI supply voltage (3.3 V)		3.135	3.3	3.465	V
$V_{DDH(1V8)}$	HDMI supply voltage (1.8 V)		1.71	1.8	1.89	V
$V_{DDI(3V3)}$	input supply voltage (3.3 V)		3.135	3.3	3.465	V
$V_{DDC(1V8)}$	core supply voltage (1.8 V)		1.71	1.8	1.89	V
$V_{DDO(3V3)}$	output supply voltage (3.3 V)		3.135	3.3	3.465	V
P	power dissipation	active mode	[2]			
		720p at 60 Hz	-	0.75	-	W
		1080p at 60 Hz	-	1.13	-	W
		1080p at 60 Hz; Deep Color mode	-	1.63	-	W
P_{cons}	power consumption	Power-down mode				
		pin PD = HIGH	-	1	-	mW
		I ² C-bus; EDID and HDCP memory power-up	-	4	-	mW
		I ² C-bus; EDID; activity detection and HDCP memory power-up	-	150	-	mW

[1] x = A, B, C or D.

[2] At 30 % activity on video port output.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDA19978AHV	HLQFP144	plastic thermal enhanced low profile quad flat package; 144 leads; body 20 × 20 × 1.4 mm; exposed die pad	SOT612-3

6. Block diagram

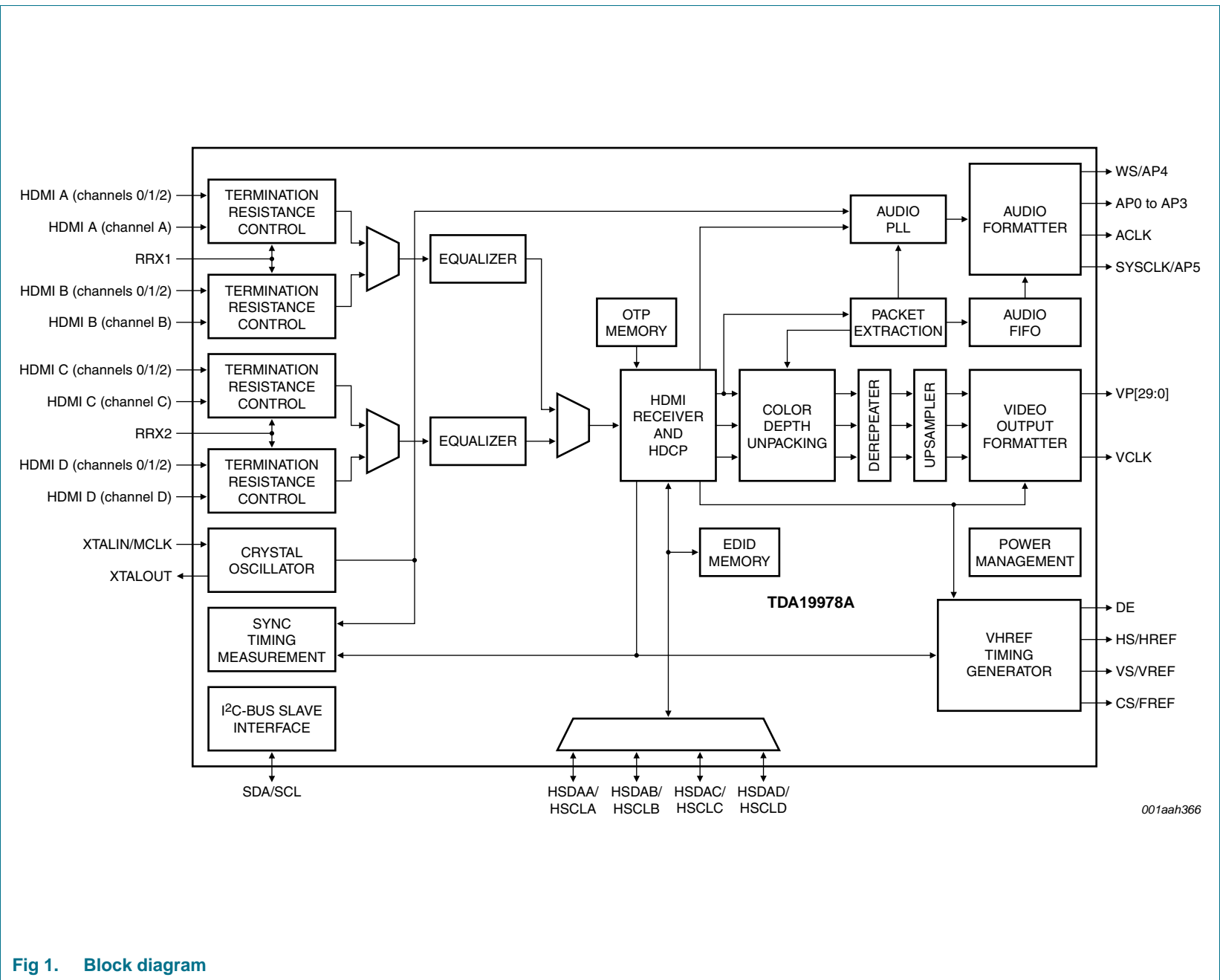


Fig 1. Block diagram

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DDx(3V3)}$	supply voltage on all 3.3 V pins		-0.5	+4.6	V
$V_{DDx(1V8)}$	supply voltage on all 1.8 V pins		-0.5	+2.5	V
ΔV_{DD}	supply voltage difference		-0.5	+0.5	V
I_O	output current		-	35	mA
T_{stg}	storage temperature		-55	+150	°C
T_{amb}	ambient temperature		0	70	°C
T_j	junction temperature		-	125	°C
V_{ESD}	electrostatic discharge voltage	HBM	-2000	+2000	V

8. Abbreviations

Table 4. Abbreviations

Acronym	Description
AVR	Audio Video Receiver
CMOS	Complementary Metal-Oxide-Semiconductor
DAC	Digital-to-Analog Converter
DDC-bus	Display Data Channel bus
DSD	Direct Stream Digital
DST	Direct Stream Transfer
DTS-HD	Digital Theater Systems HD
DVD	Digital Versatile Disc
DVI	Digital Video Interface
EDID	Extended Display Identification Data
HBM	Human Body Model
HBR	High-Bitrate
HD	High-Definition
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface
HDTV	High-Definition TeleVision
LV-TTL	Low Voltage Transistor-Transistor Logic
OTP	One Time Programmable
PLL	Phase-Locked Loop
RGB	Red Green Blue
SACD	Super Audio CD
S/PDIF	Sony/Philips Digital Interface Format
SYNC	SYNChronization
TMDS	Transition Minimized Differential Signaling
UXGA	Ultra eXtended Graphics Array

Table 4. Abbreviations ...continued

Acronym	Description
VHREF	Vertical Horizontal REFerence
VGA	Video Graphics Array
WUXGA	Wide Ultra eXtended Graphics Array
YCbCr	Y = Luminance, Cb = Chroma blue, Cr = Chroma red

9. Revision history

Table 5. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA19978A_SDS v.4	20101206	Product data sheet	-	TDA19978A_SDS v.3
Modifications:	<ul style="list-style-type: none"> • Replaced in all document HDMI 1.3a with HDMI 1.4a • Replaced in all document HDCP 1.2 with HDCP 1.4 			
TDA19978A_SDS v.3	20100511	Product data sheet	-	TDA19978A_SDS v.1 ^[1]
TDA19978A_SDS v.1	20080528	Objective data sheet	-	-

[1] Revision 2 is not available.

10. Legal information

10.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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12. Contents

1	General description	1
2	Features and benefits	2
3	Applications	3
4	Quick reference data	3
5	Ordering information	4
6	Block diagram	5
7	Limiting values	6
8	Abbreviations	6
9	Revision history	7
10	Legal information	8
10.1	Data sheet status	8
10.2	Definitions	8
10.3	Disclaimers	8
10.4	Licenses	9
10.5	Trademarks	9
11	Contact information	9
12	Contents	10

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